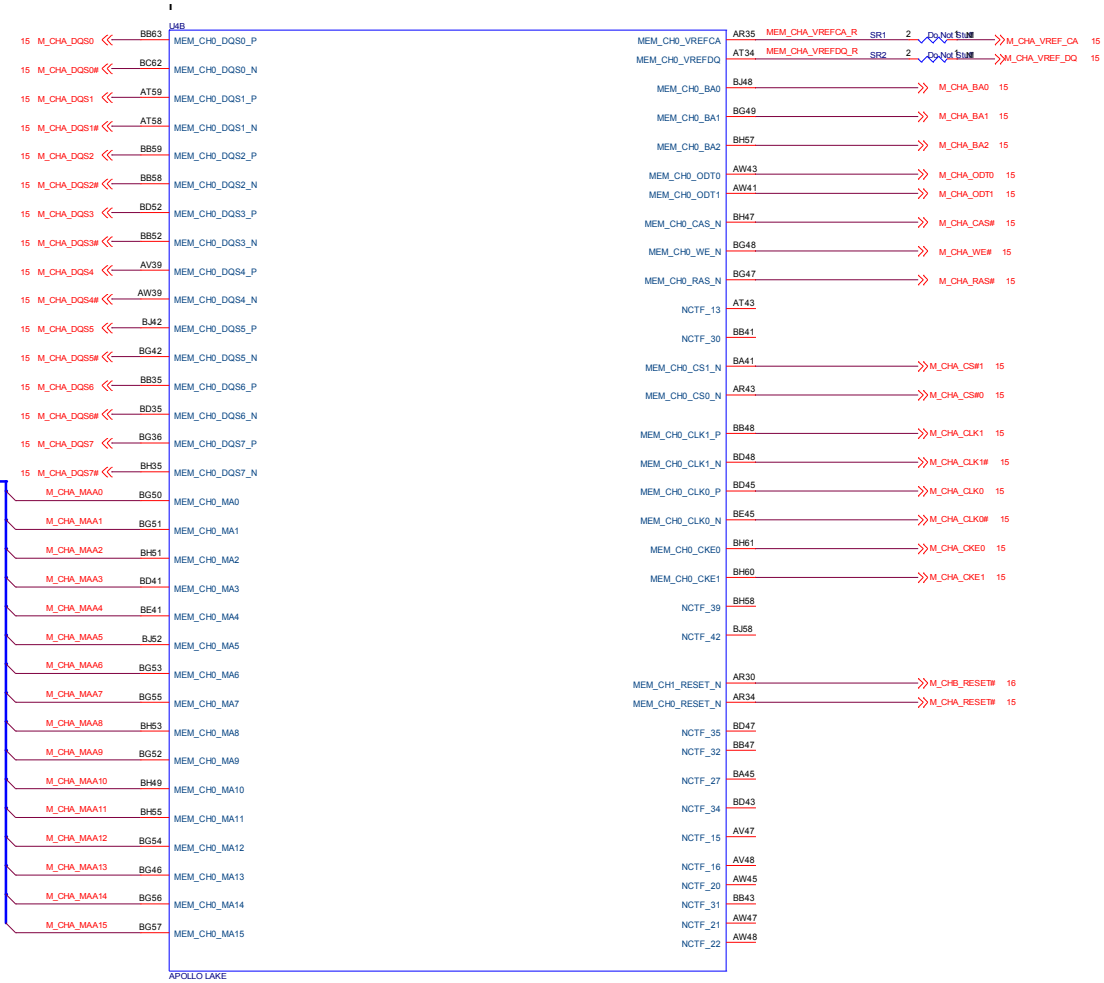
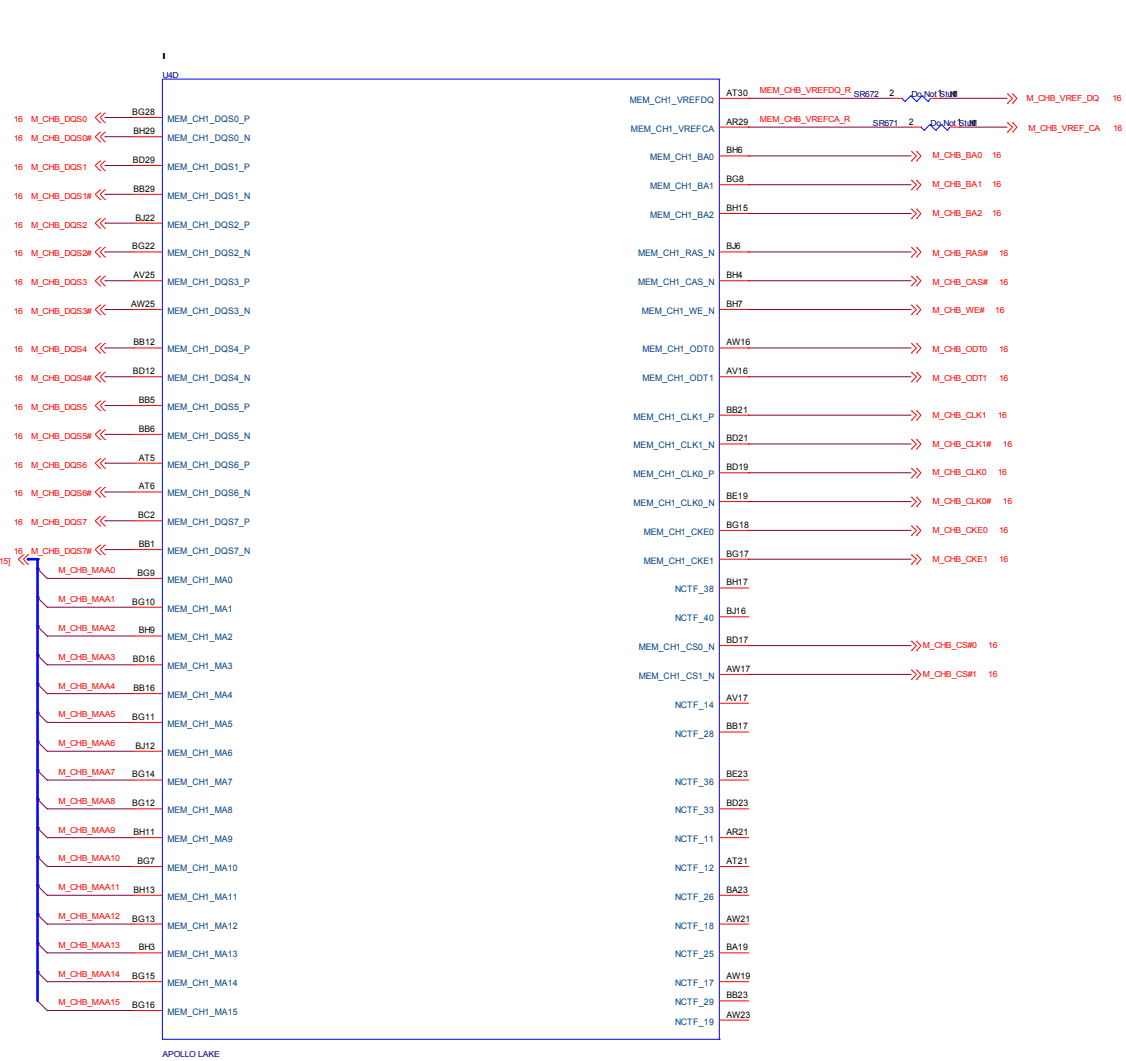
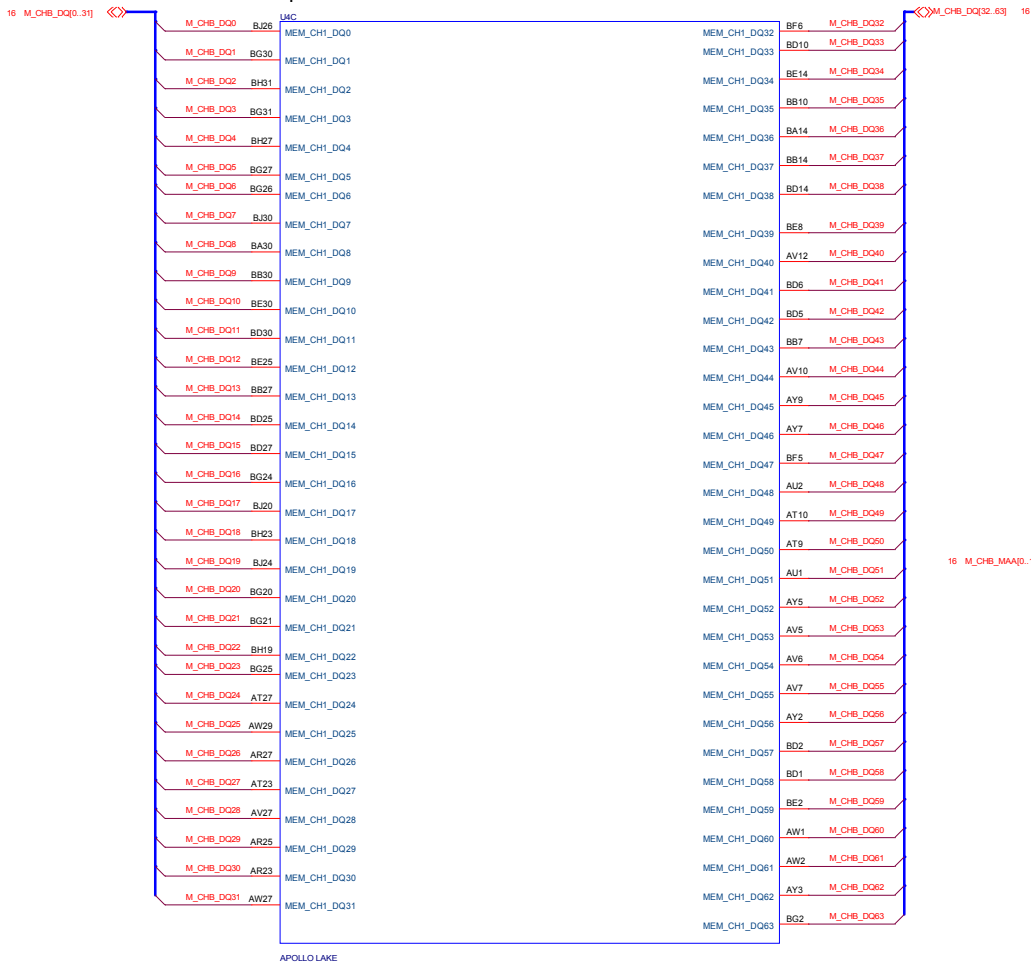
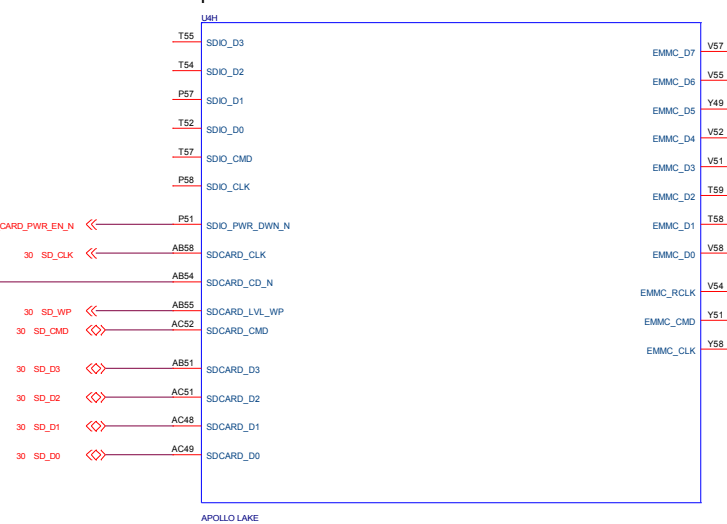
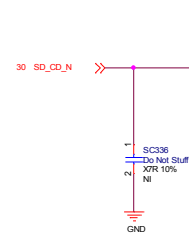
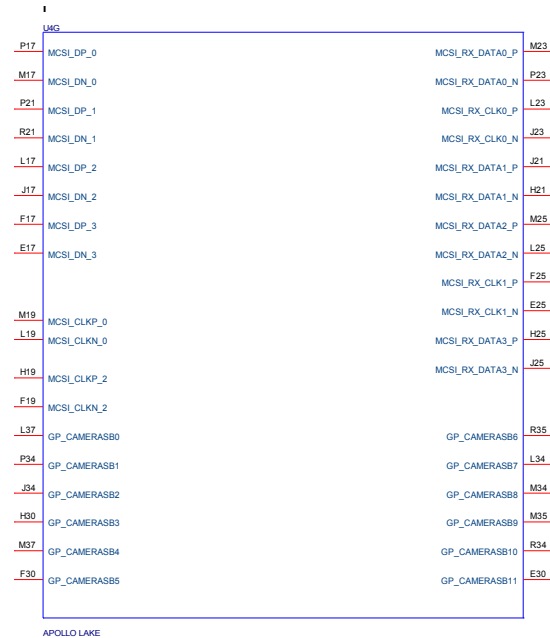
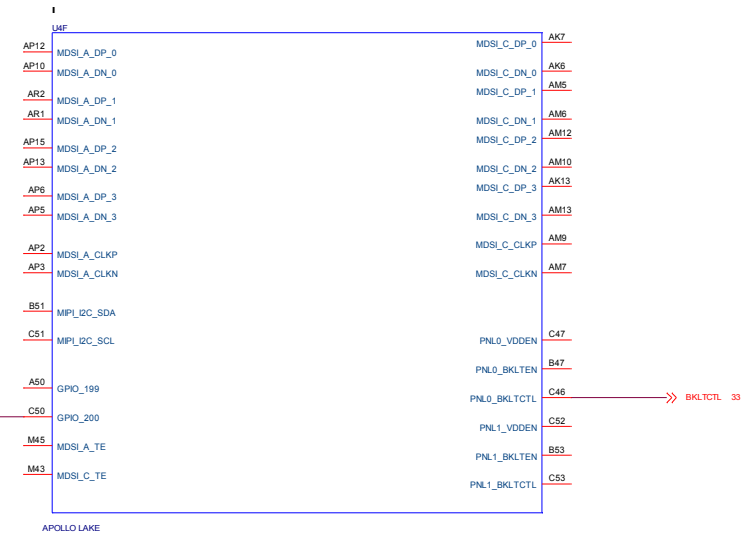
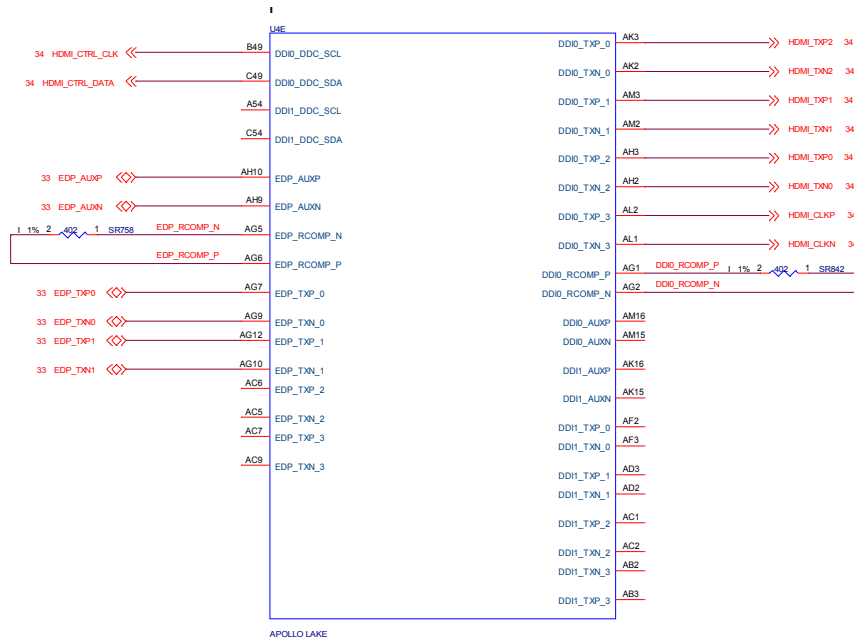
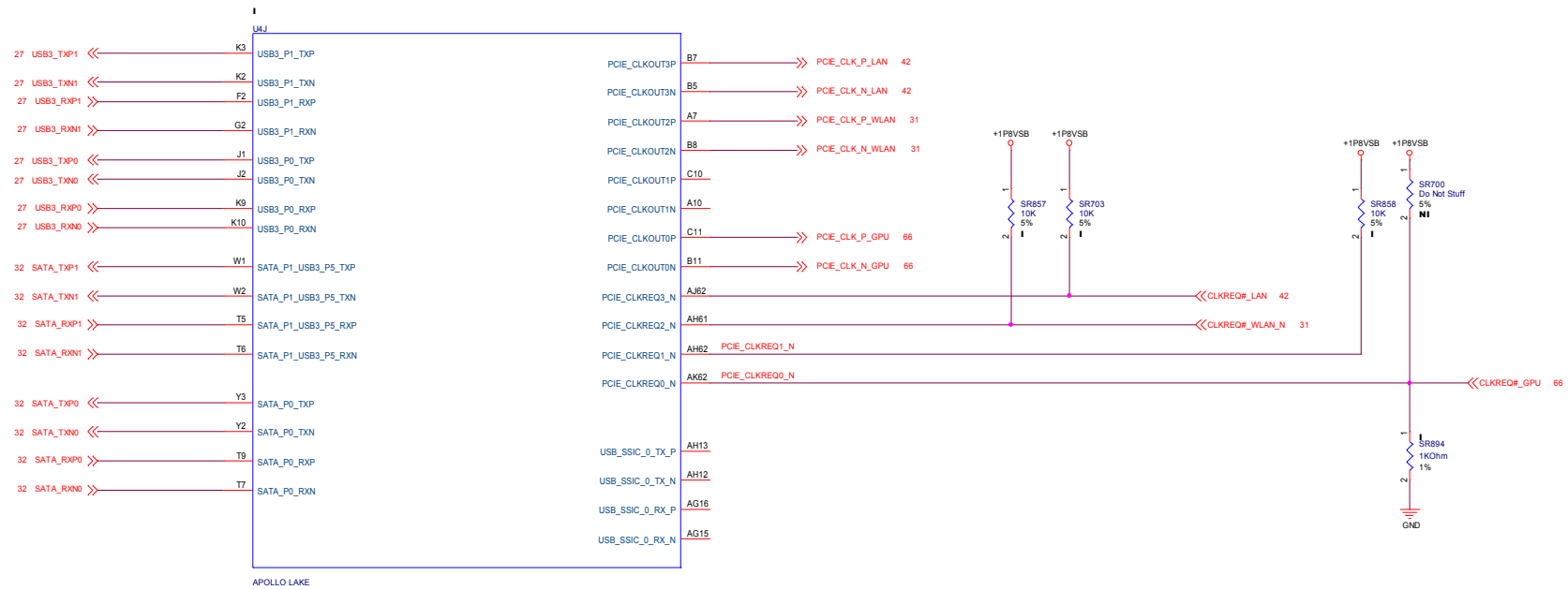
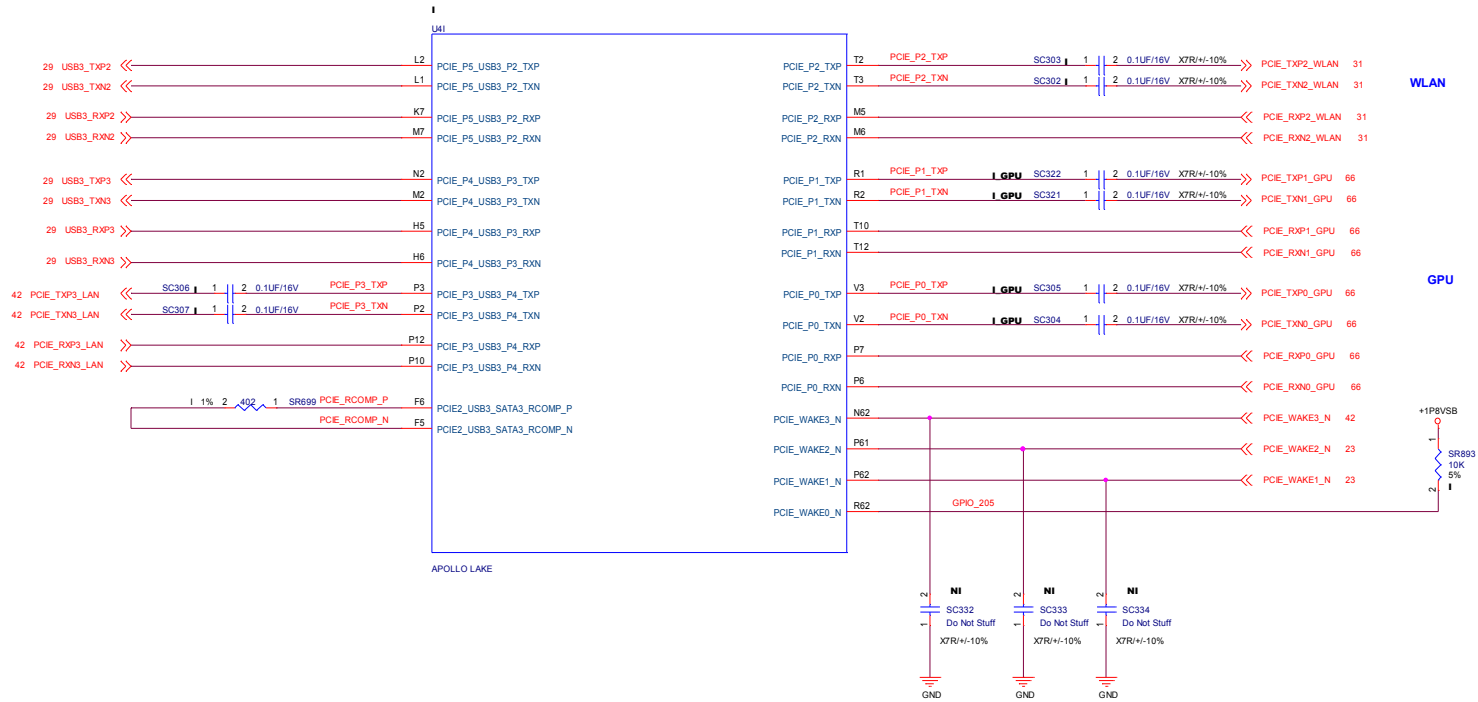


15 M\_CHA\_MAA[0..15]



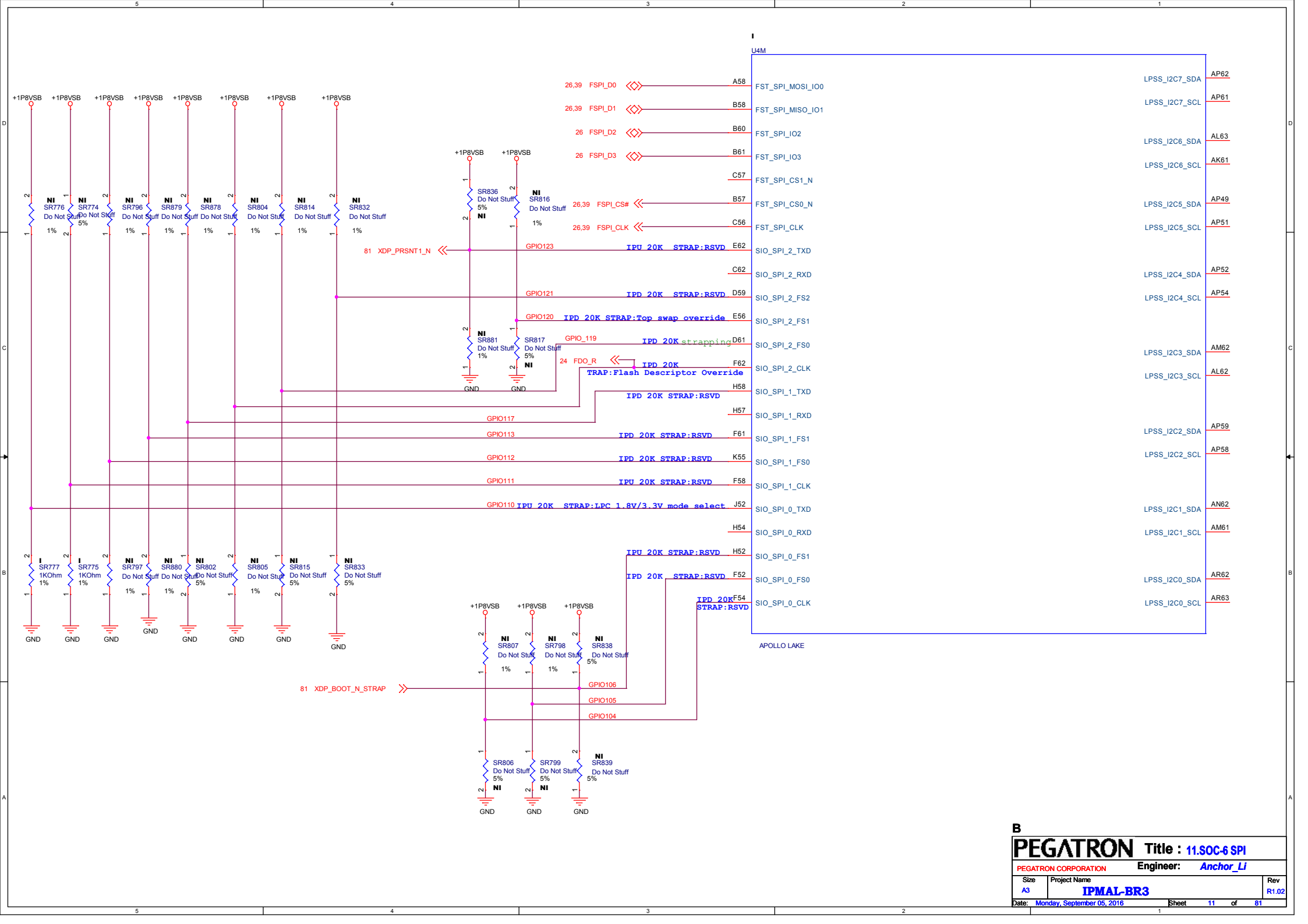




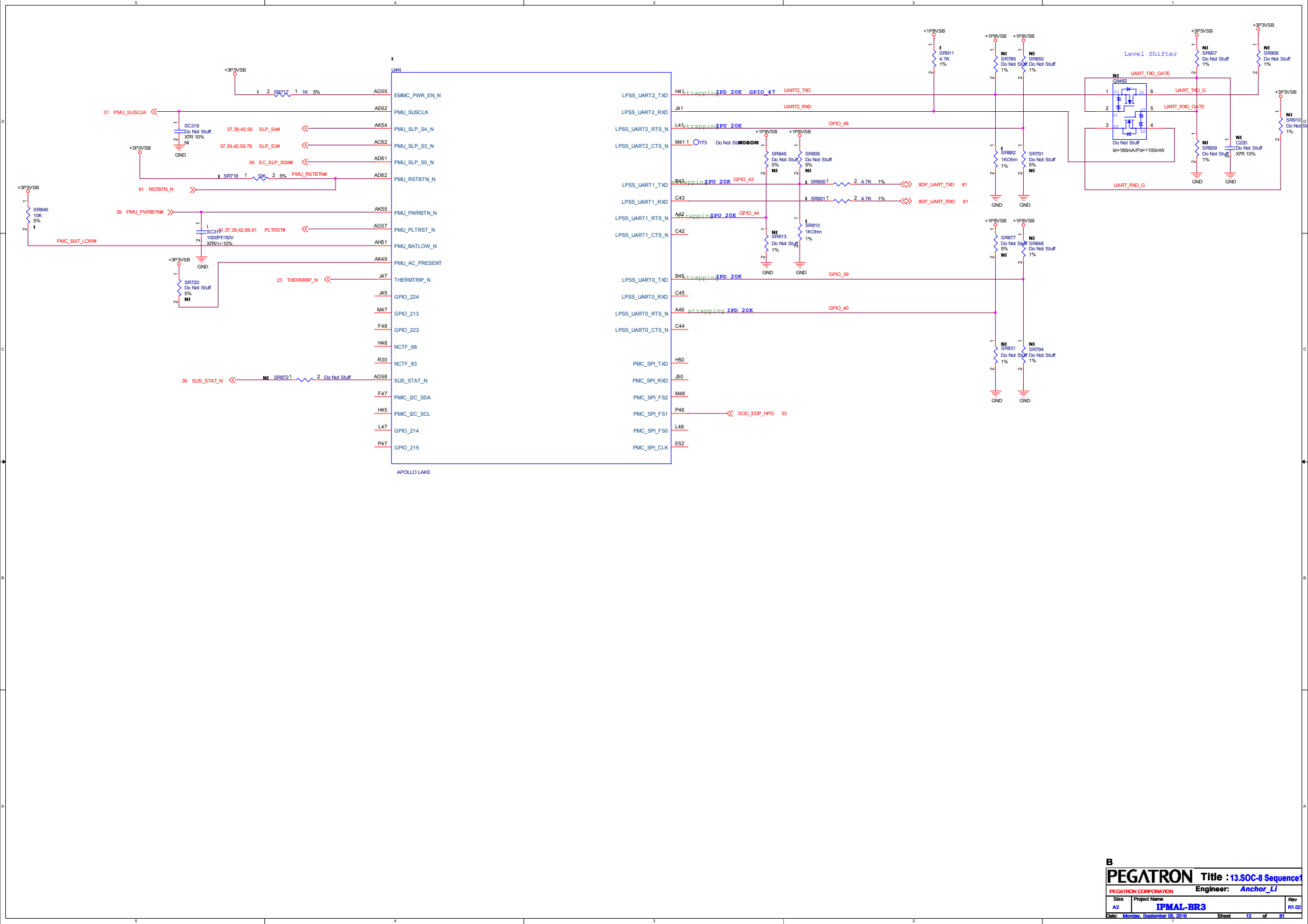


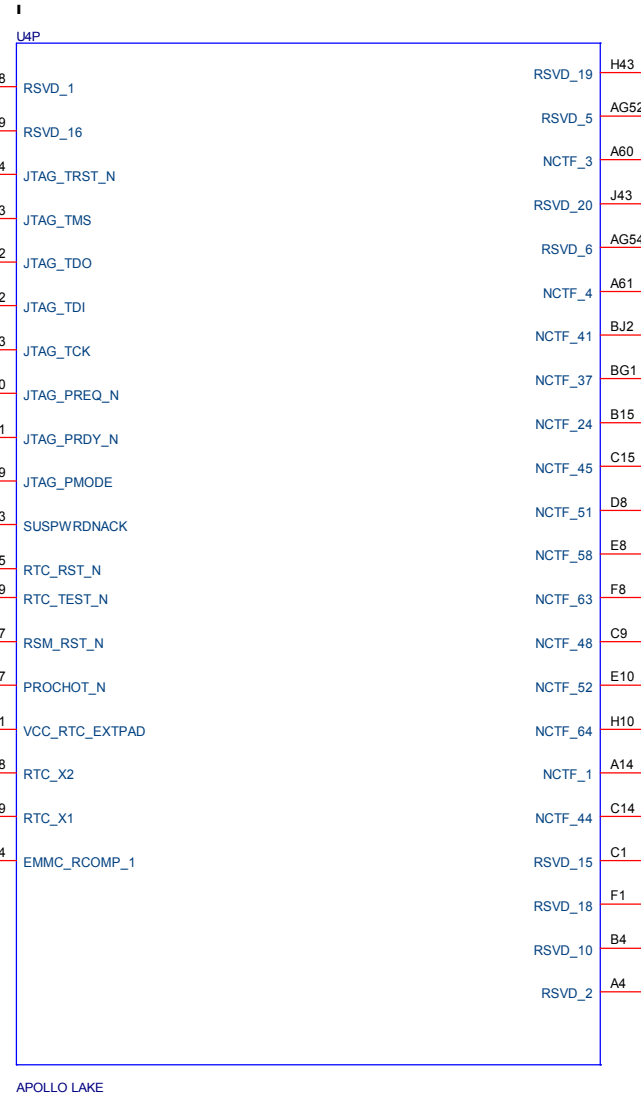
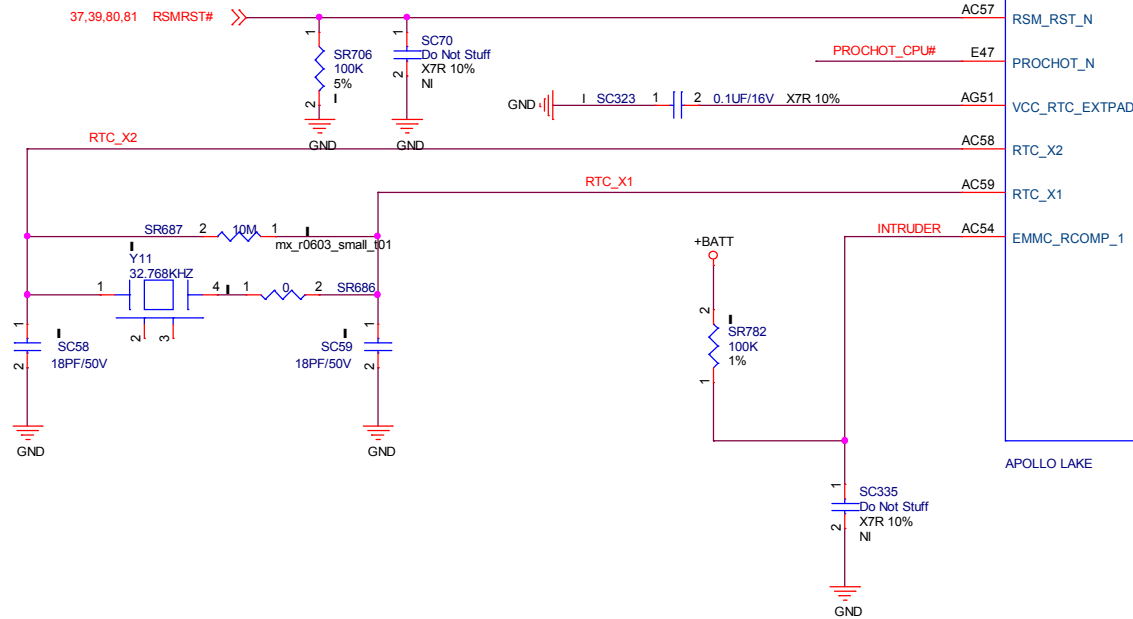
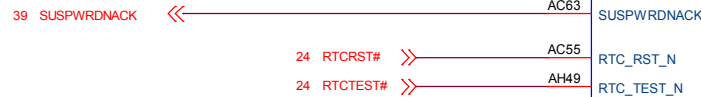
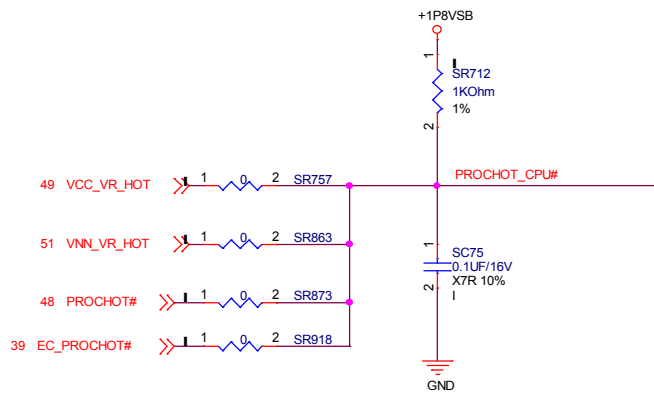






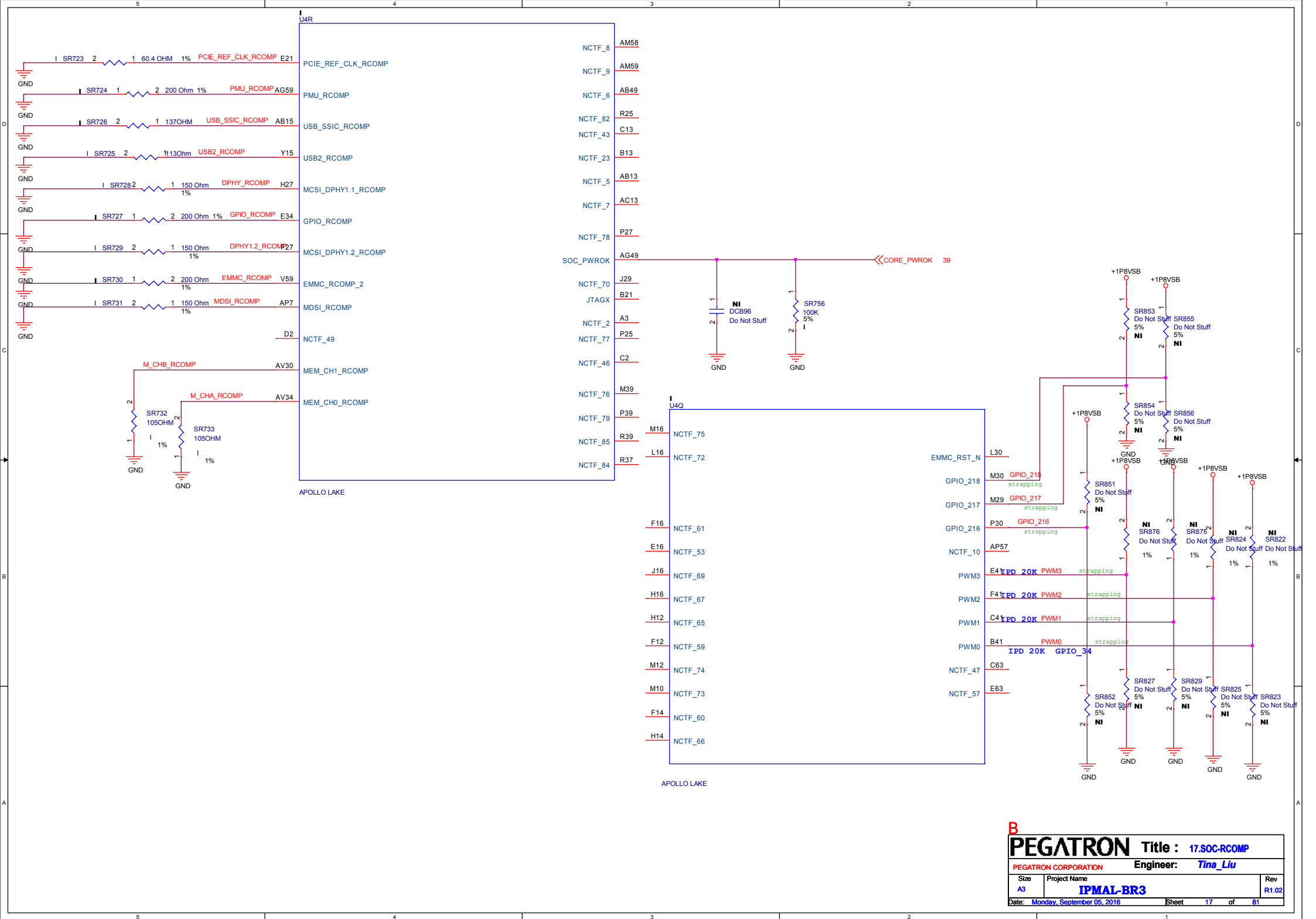


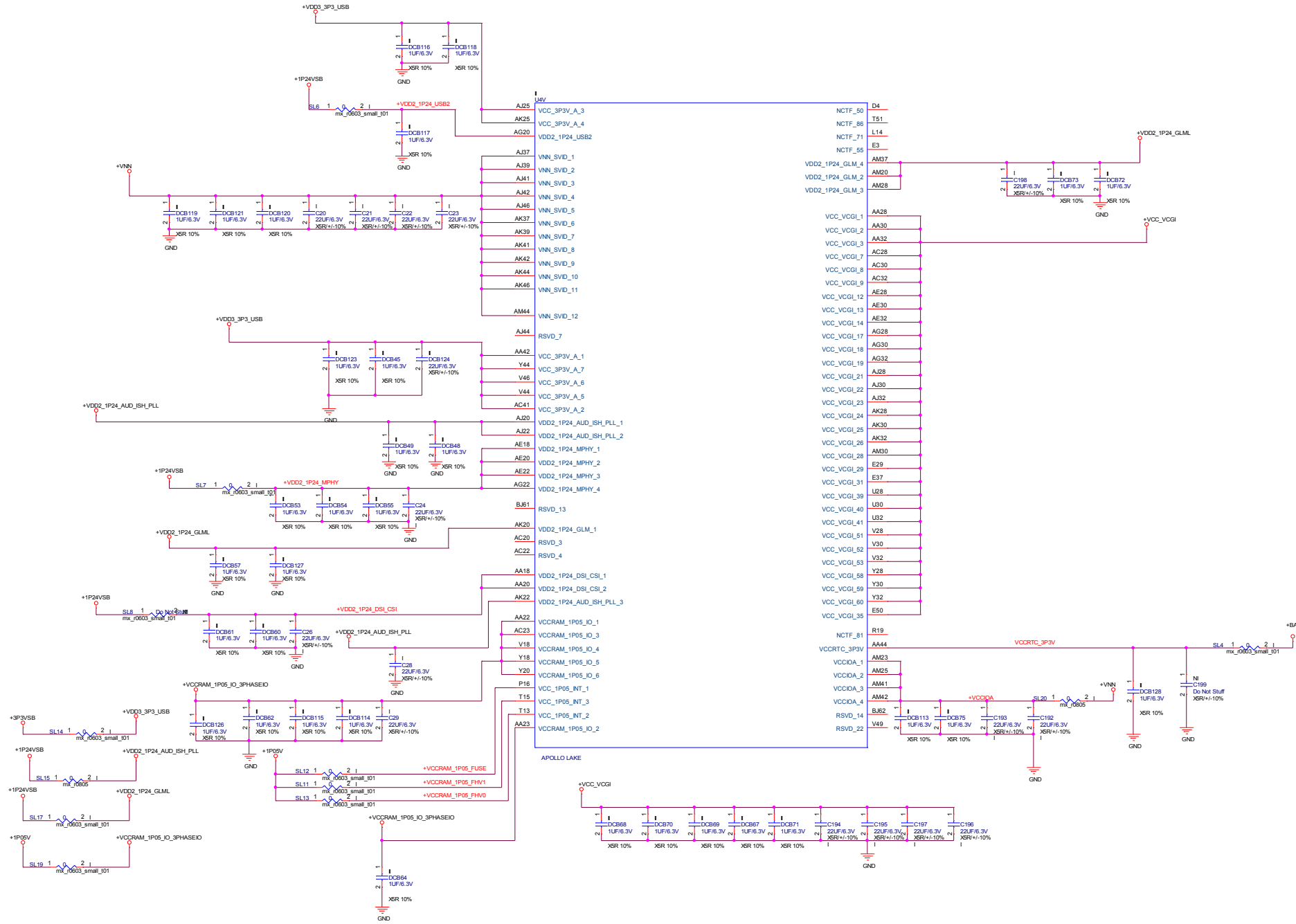




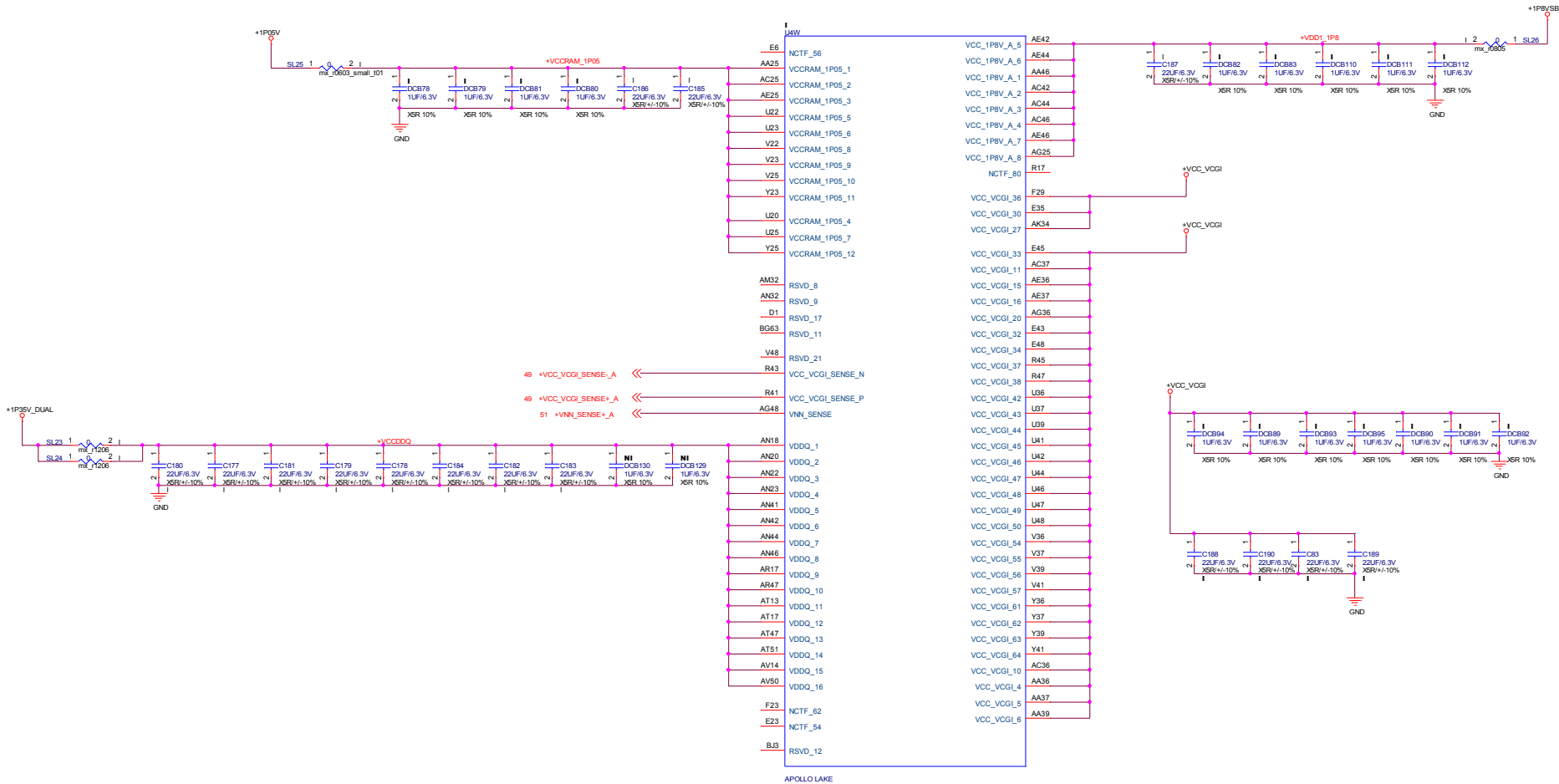


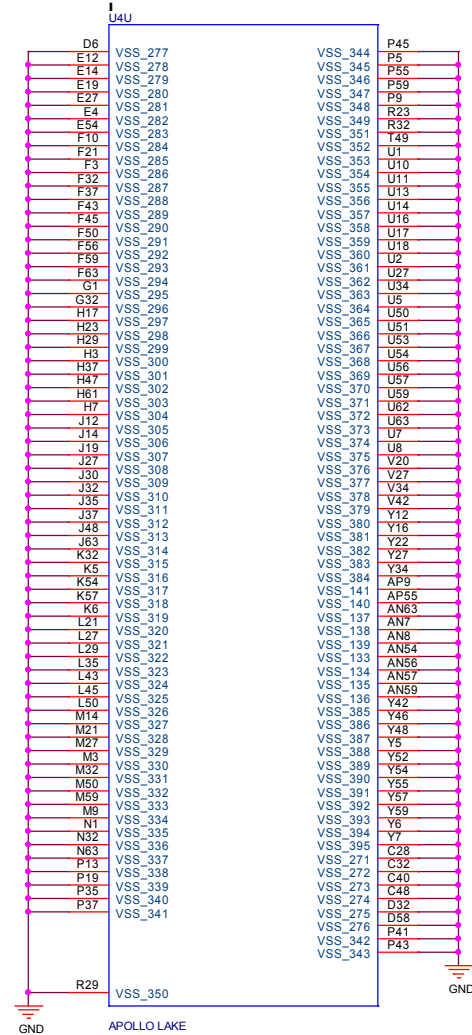
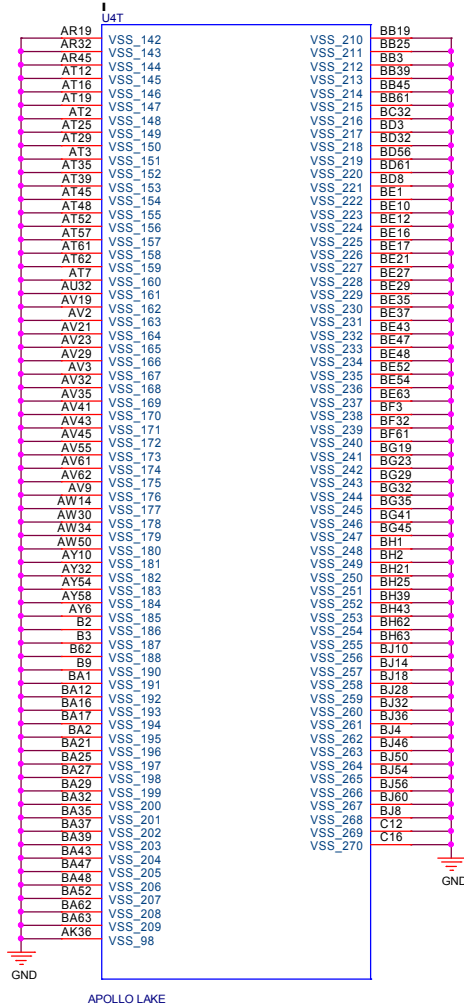
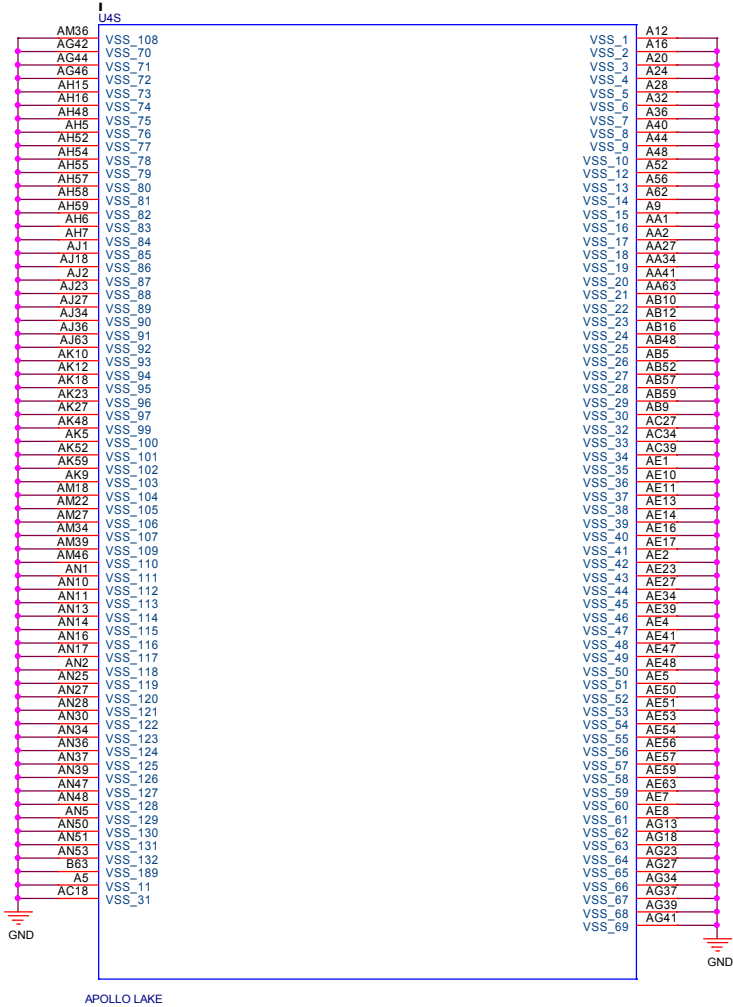


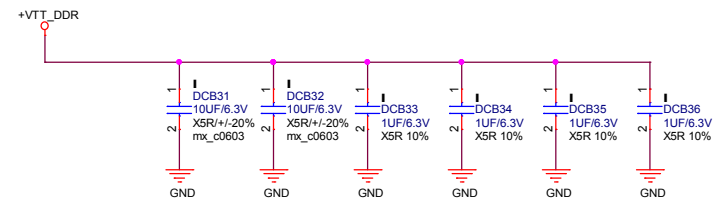
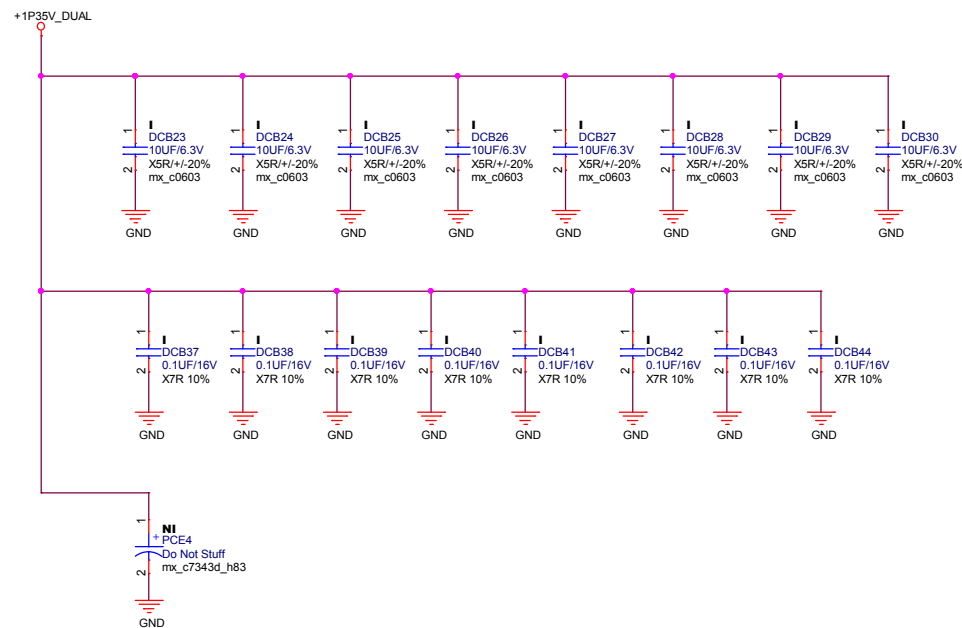
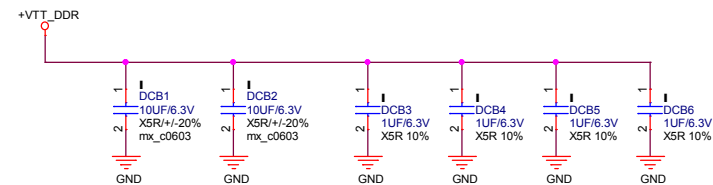
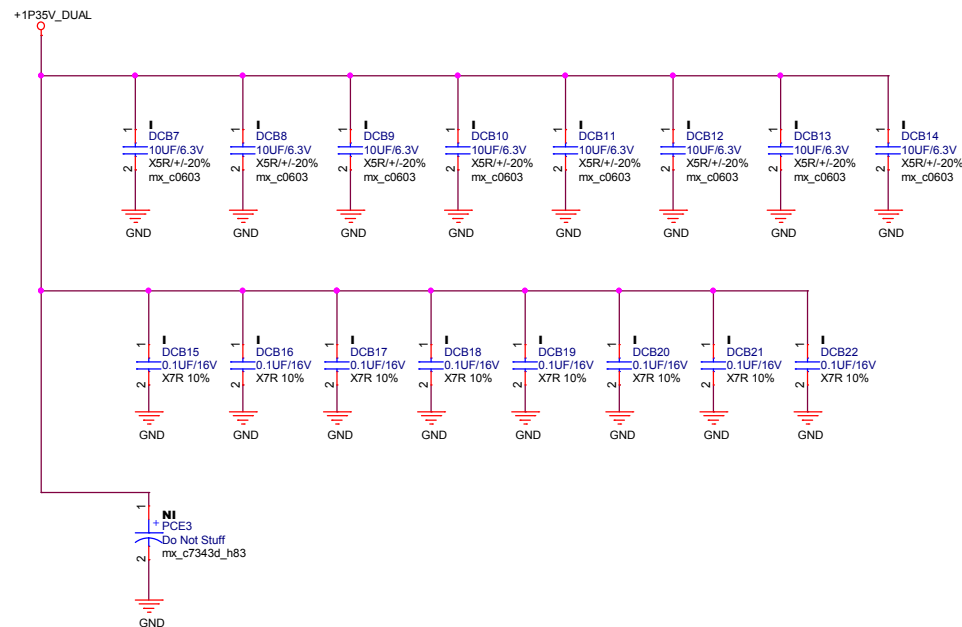






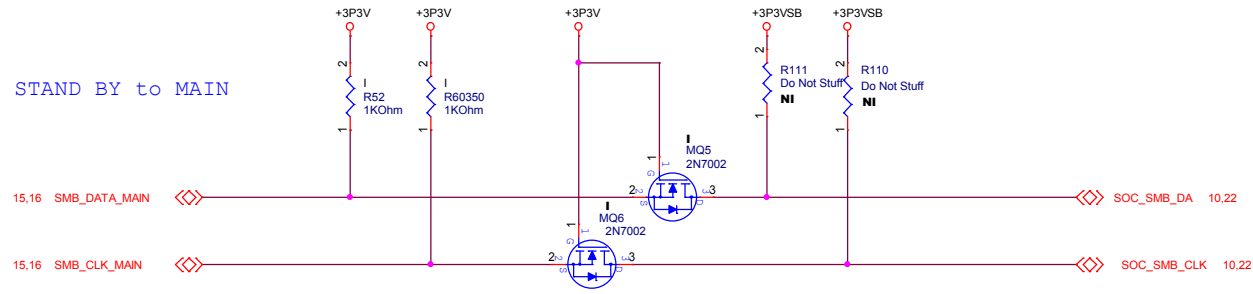




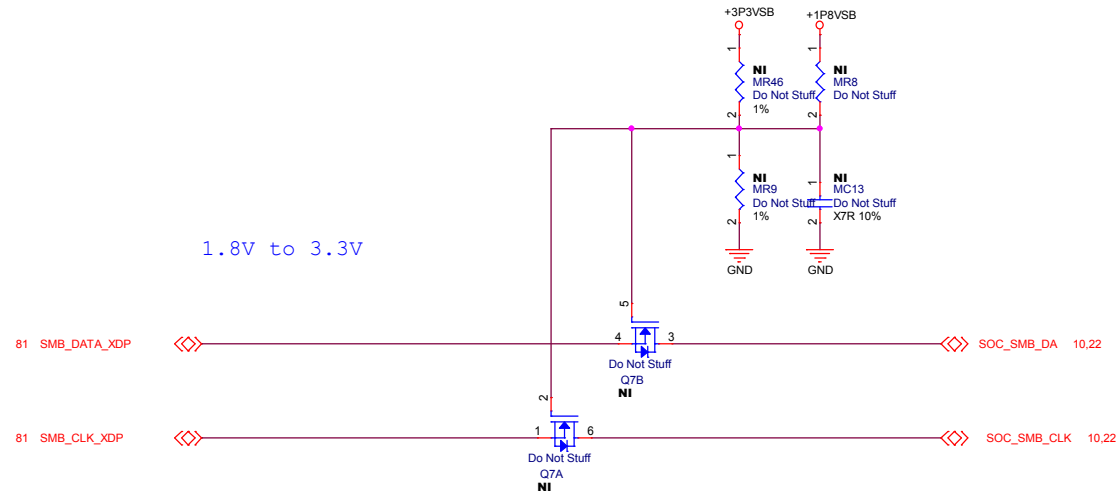


# PCH SMBus

STAND BY to MAIN



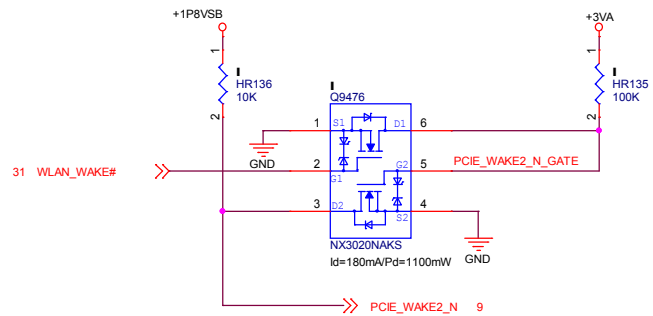
1.8V to 3.3V



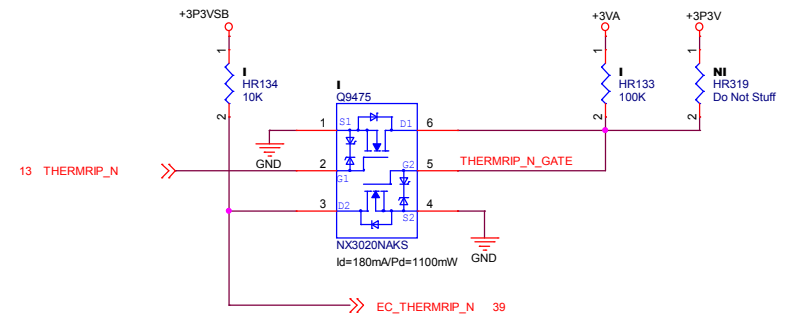
B

|                                  |                                  |                                  |  |
|----------------------------------|----------------------------------|----------------------------------|--|
| <b>PEGATRON</b>                  |                                  | Title : 22. SOC-CONTROL SIGNAL-1 |  |
| PEGATRON CORPORATION             |                                  | Engineer: <i>Anchor_Li</i>       |  |
| Size<br>A3                       | Project Name<br><b>IPMAL-BR3</b> | Rev<br>R1.02                     |  |
| Date: Monday, September 05, 2016 |                                  | Sheet 22 of 81                   |  |

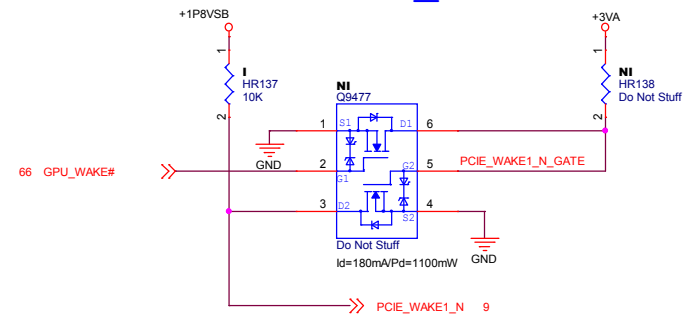
## LAN WAKE#



## THERMRIP



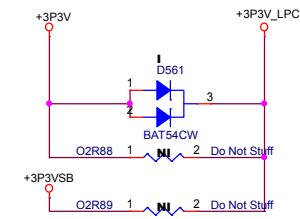
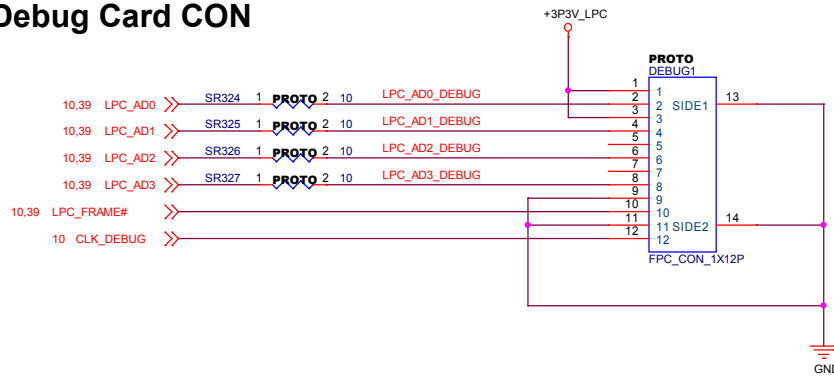
## GPU\_WAKE#



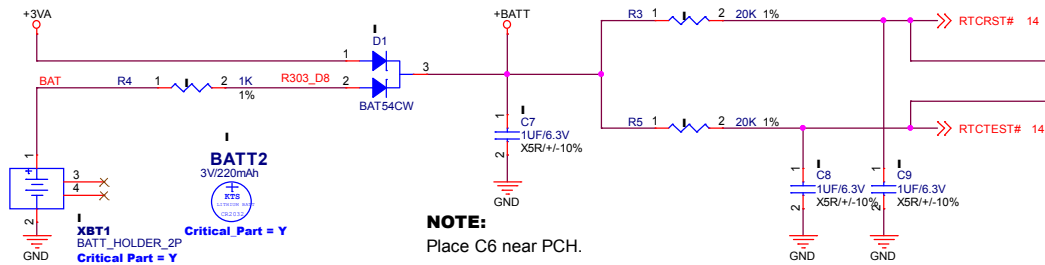
B

|                                  |                                  |                                 |              |
|----------------------------------|----------------------------------|---------------------------------|--------------|
| <b>PEGATRON</b>                  |                                  | Title : 23.SOC-CONTROL SIGNAL-2 |              |
| PEGATRON CORPORATION             |                                  | Engineer: Anchor_Li             |              |
| Size<br>A3                       | Project Name<br><b>IPMAL-BR3</b> |                                 | Rev<br>R1.02 |
| Date: Monday, September 05, 2016 |                                  | Sheet                           | 23 of 61     |

## Debug Card CON

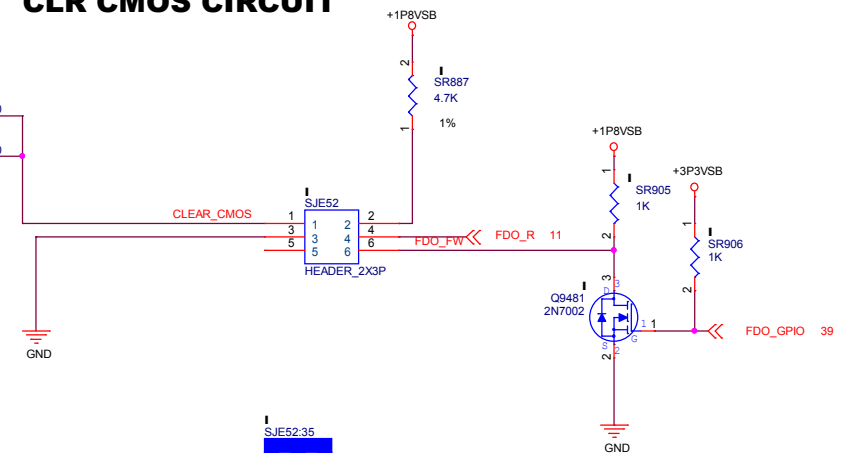


## External RTC Circuitry



| ME Settings |           |
|-------------|-----------|
| Enable ME   | 4 6 Short |
| disable ME  | 2 4 Open  |

## CLR CMOS CIRCUIT

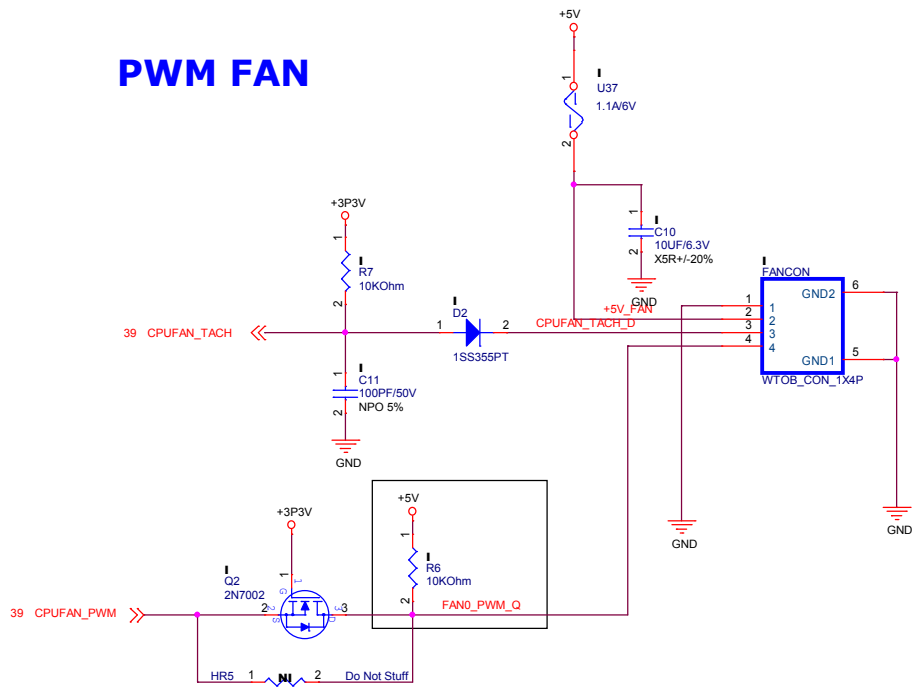


| CMOS RTC |         |
|----------|---------|
| 3-5      | DEFAULT |
| 1-3      | CLEAR   |

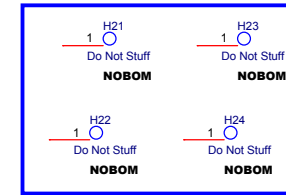
PEGATRON DT-MB RESTRICTED SECRET

|                                  |                        |                                   |           |
|----------------------------------|------------------------|-----------------------------------|-----------|
| <b>PEGATRON</b>                  |                        | Title : 24.RTC/LPC DEBUG/CLR CMOS |           |
| PEGATRON CORPORATION             |                        | Engineer: Anchor_Li               |           |
| Size A3                          | Project Name IPMAL-BR3 |                                   | Rev R1.02 |
| Date: Monday, September 05, 2016 |                        | Sheet 24 of 81                    |           |

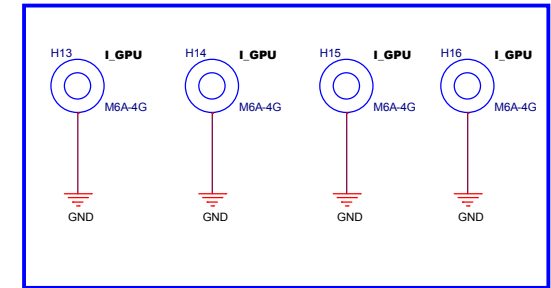
## PWM FAN



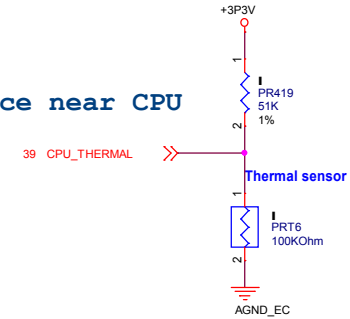
## NUTS for Thermal (CPU)



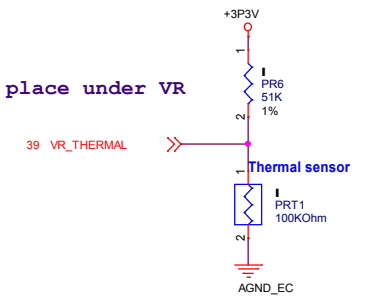
### NUTS for Thermal (GPU)



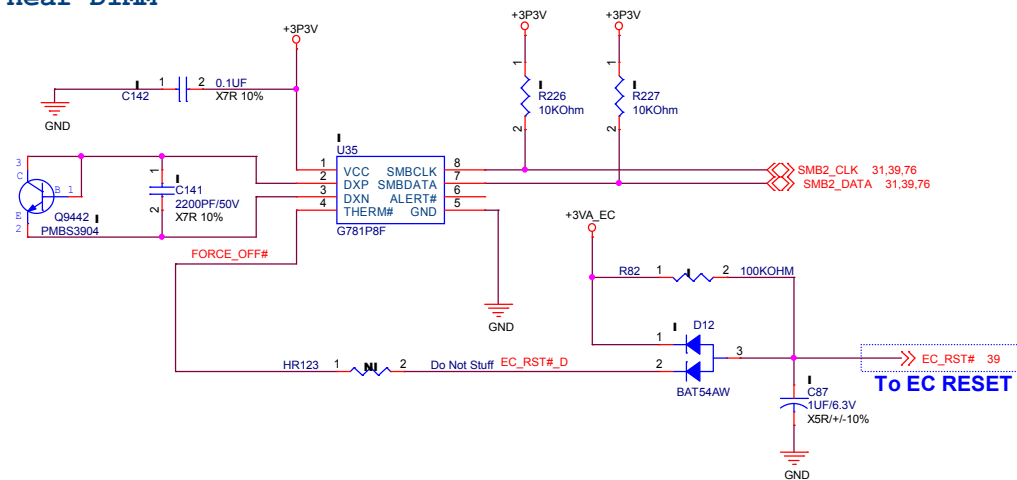
place near CPU



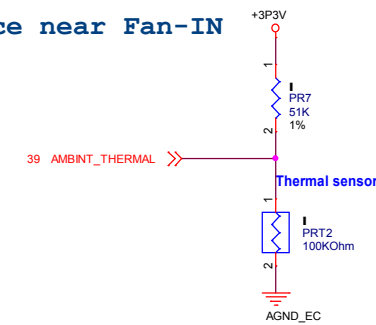
place under VR



place near DIMM



place near Fan-IN

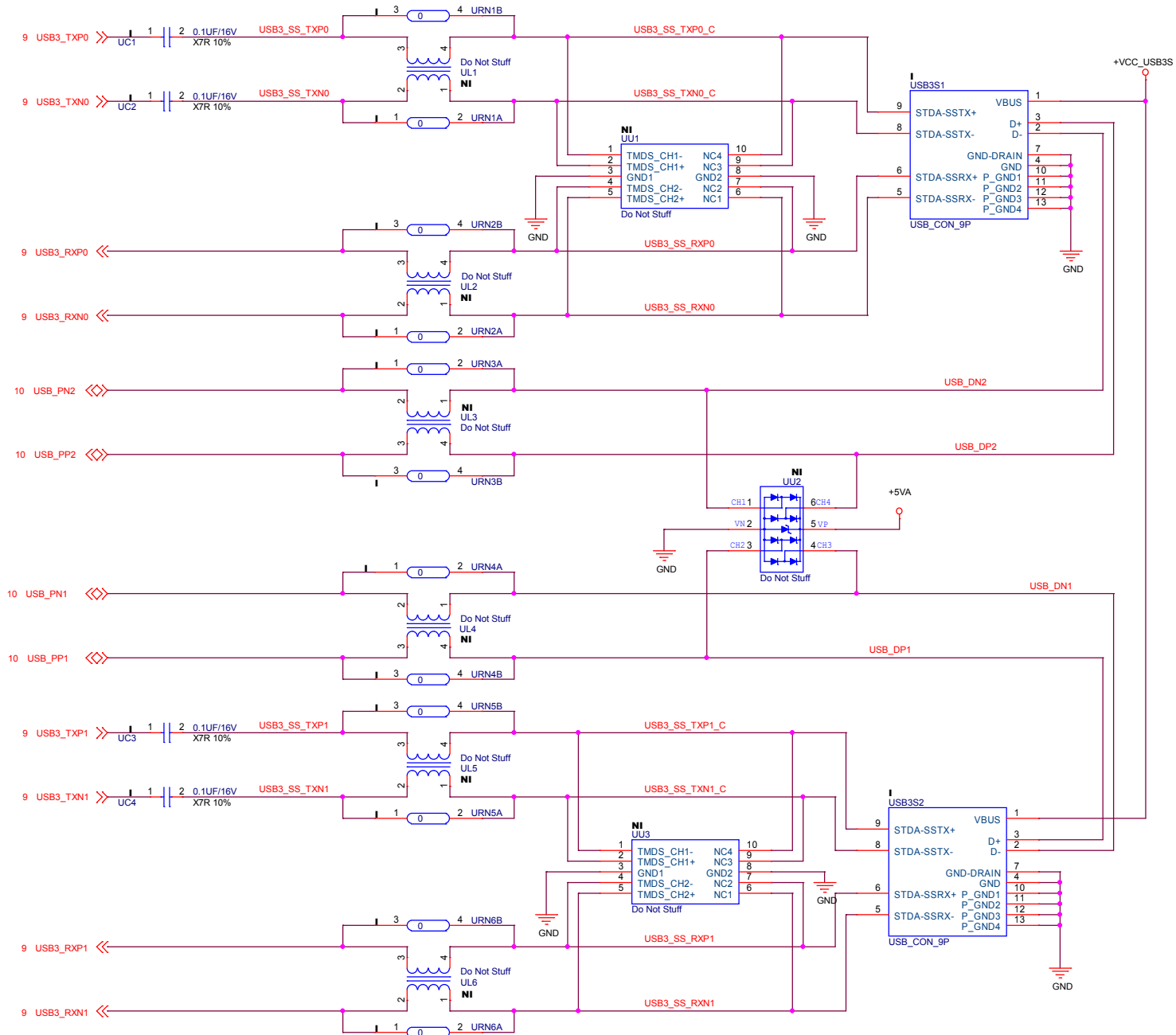


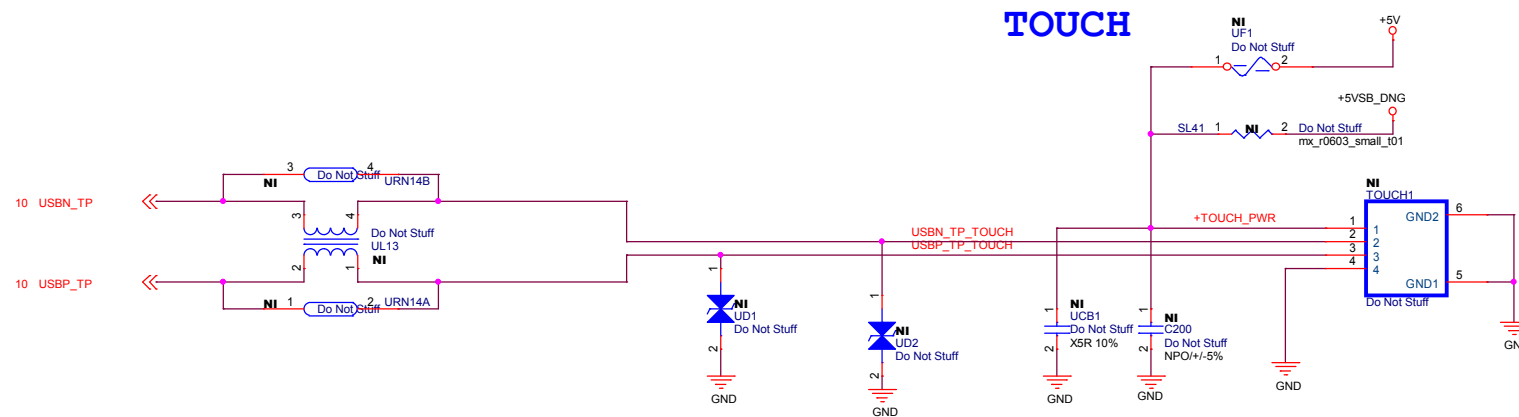
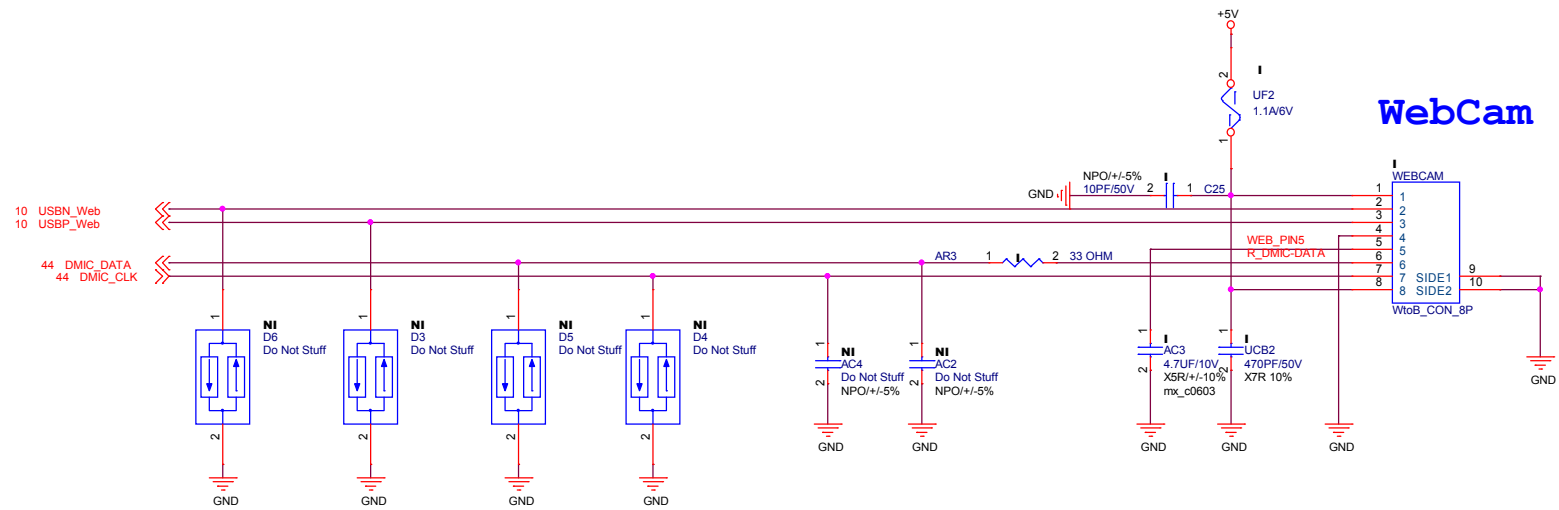
|   |   |                     |                              |
|---|---|---------------------|------------------------------|
| <b>PEGATRON</b>                         |   | <b>Title :</b>      | 25.FAN/HEATSINK/ThermaSensor |
| <b>PEGATRON CORPORATION</b>             |   | <b>Engineer:</b>    | Anchor_Li                    |
| <b>Size</b><br>A3                       | <b>Project Name</b><br><b>IPMAL-BR3</b> | <b>Rev</b><br>R1.02 |                              |
| <b>Date:</b> Monday, September 05, 2016 |   | <b>Sheet</b>        | 25 of 81                     |



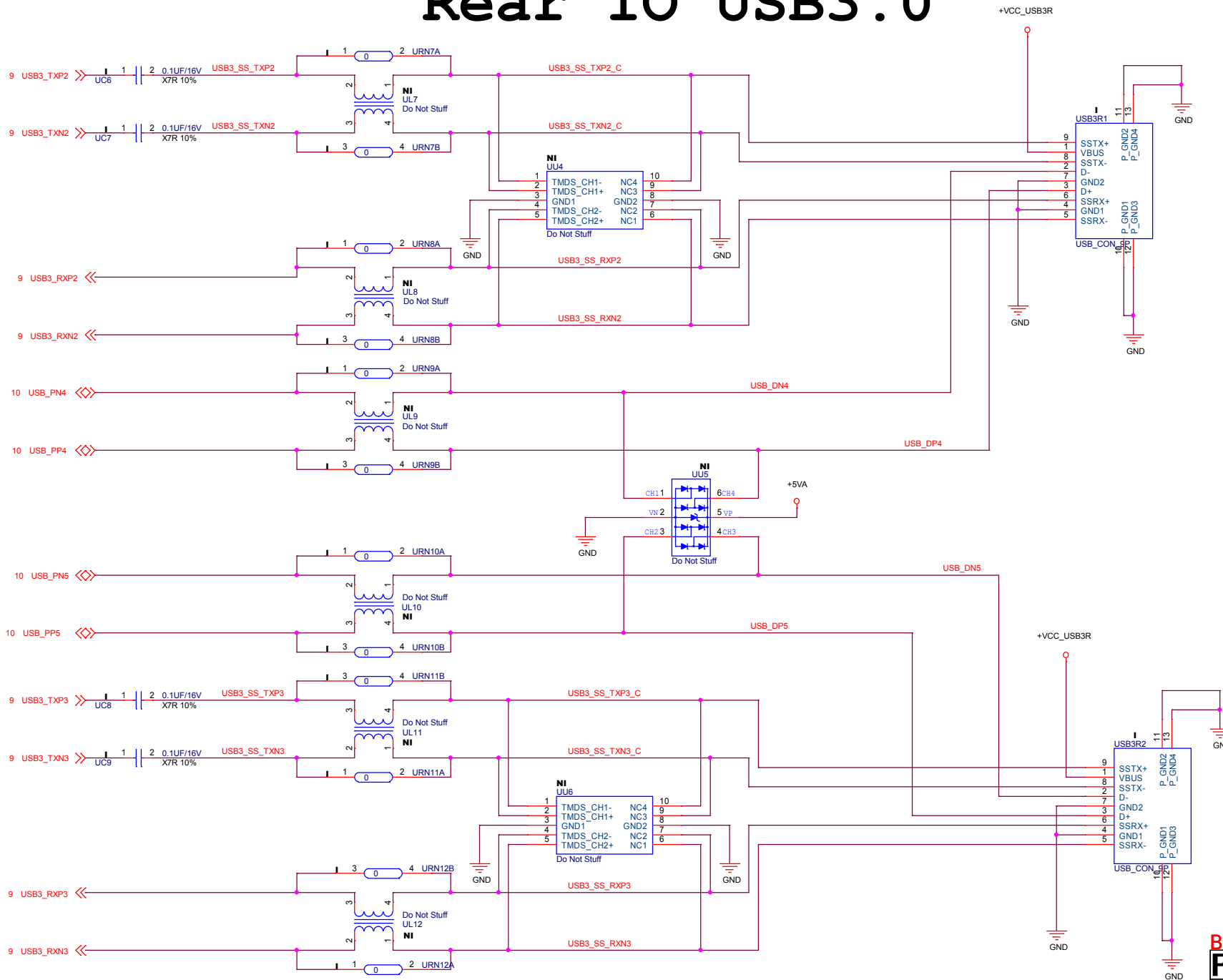


# Side IO USB3.0

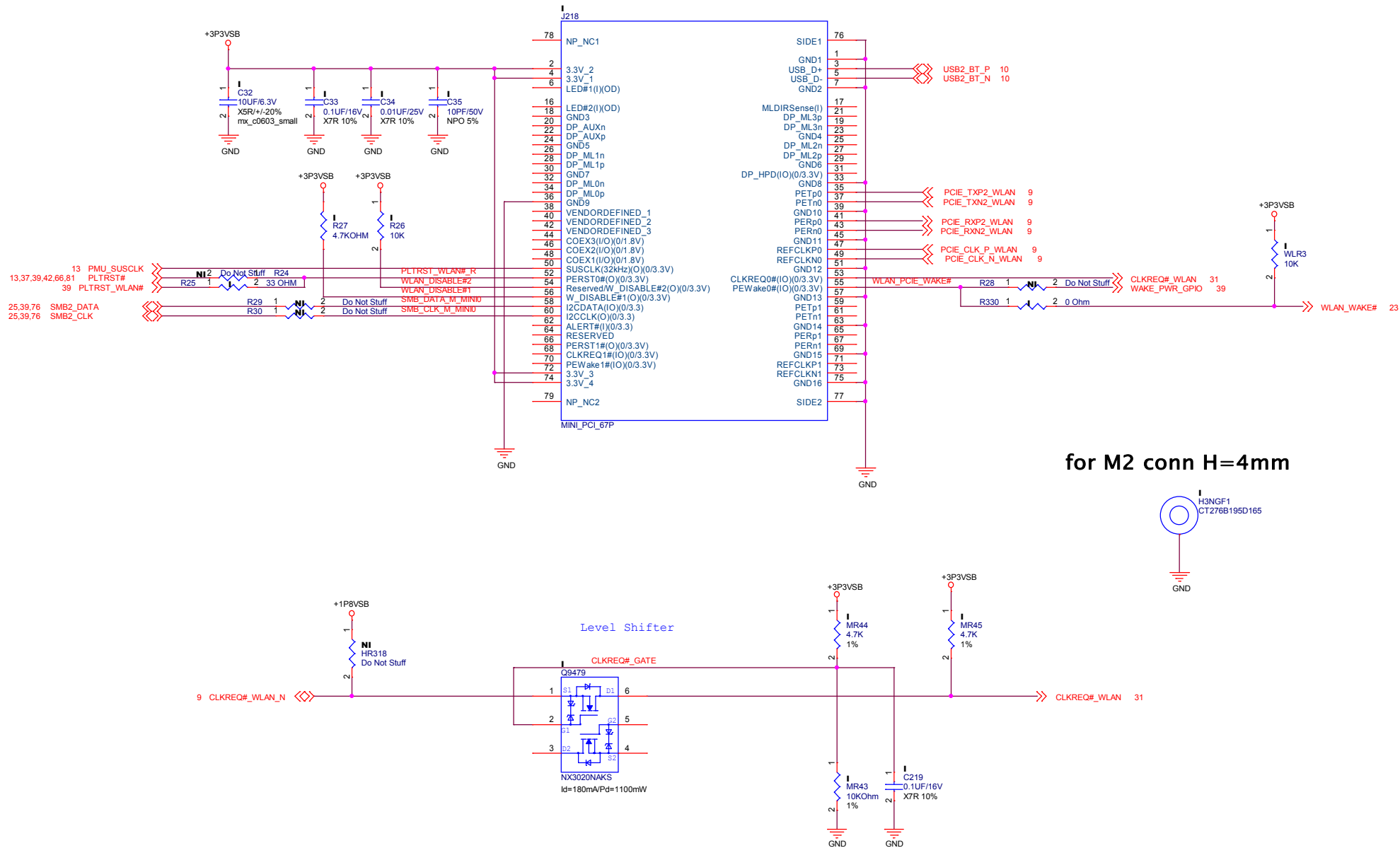




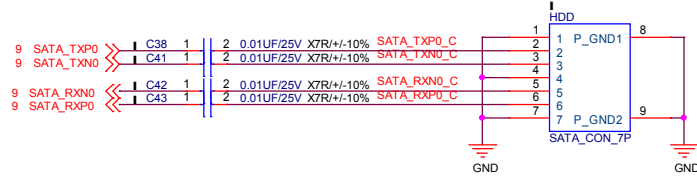
# Rear IO USB3.0





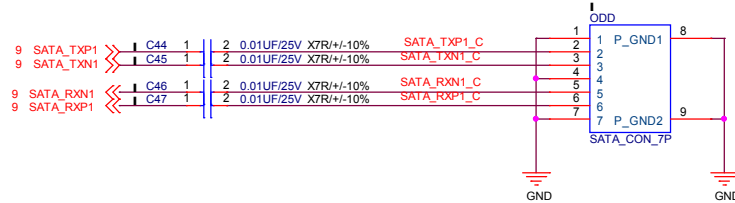


## SATA HDD CON



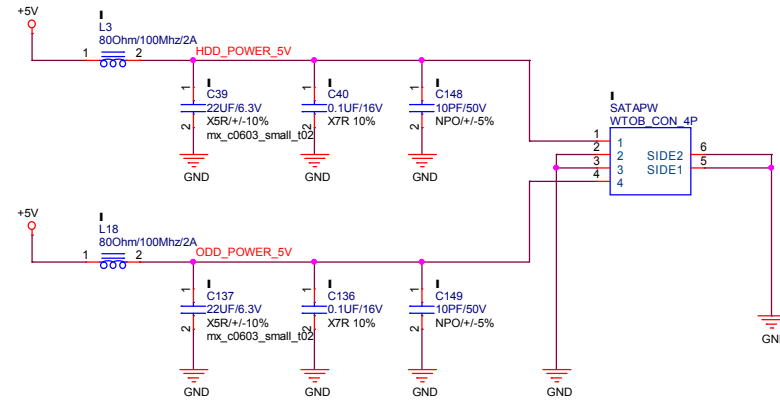
**SATA CONTROLLER #1  
(MASTER)  
COLOR = DARK BLUE**

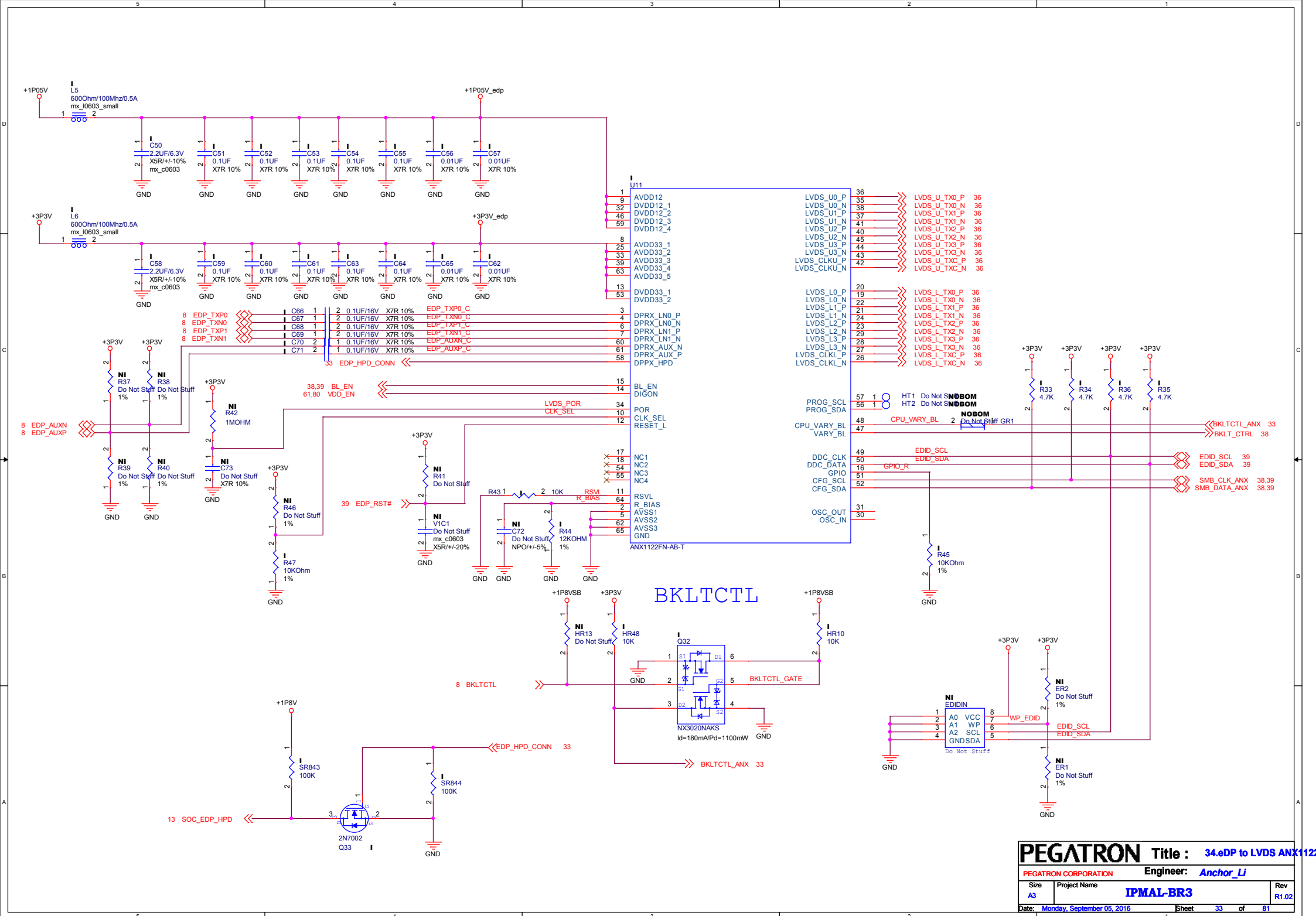
## SATA ODD CON



**SATA CONTROLLER #2  
(SLAVE)**

## SATA POWER CONN FOR HDD/ODD

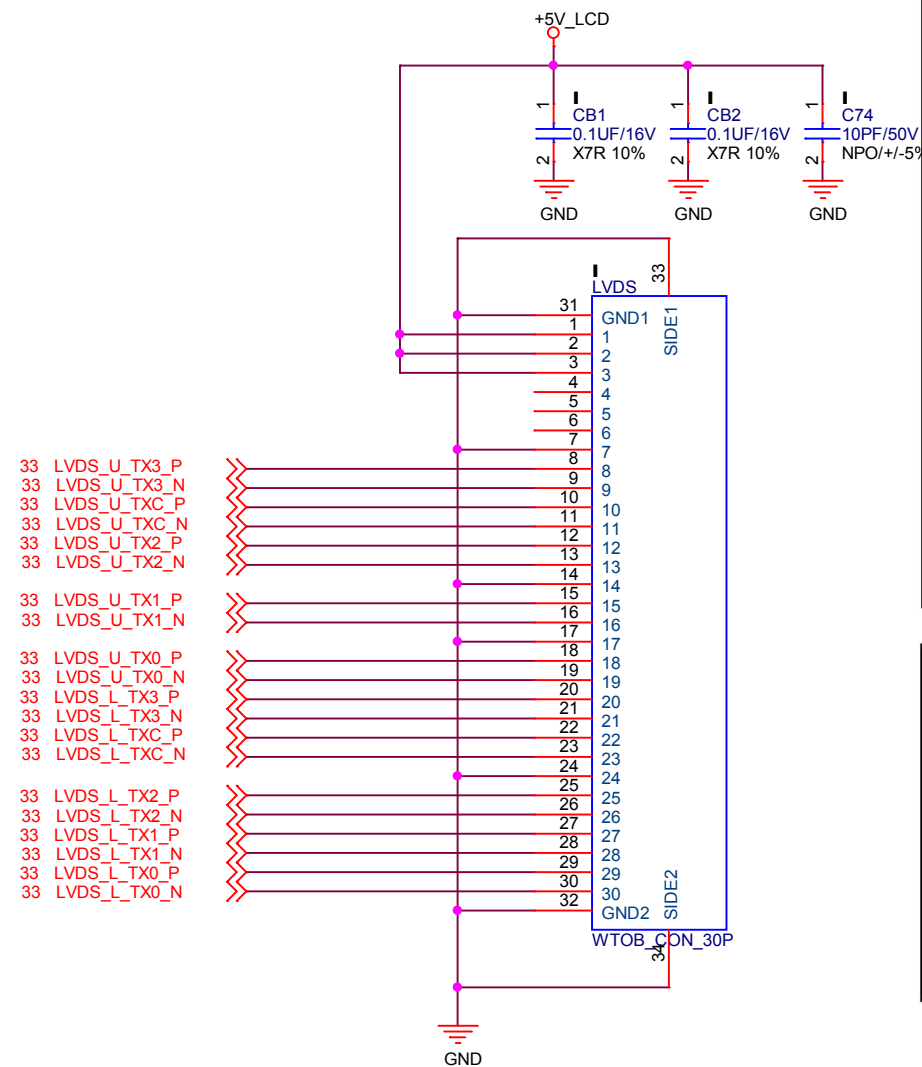








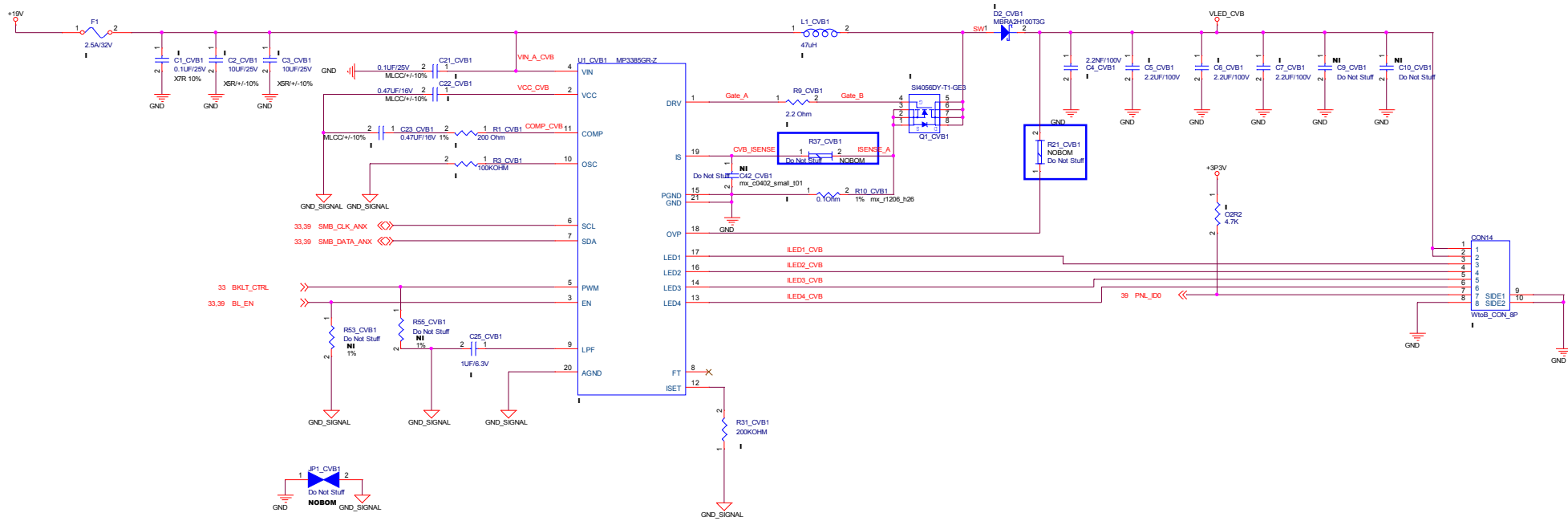




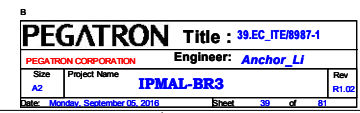
| Pin | Name  | Description  |
|-----|-------|--|
| 1   | RXO0- | Negative LVDS differential data input. Channel O0 (odd)  |
| 2   | RXO0+ | Positive LVDS differential data input. Channel O0 (odd)  |
| 3   | RXO1- | Negative LVDS differential data input. Channel O1 (odd)  |
| 4   | RXO1+ | Positive LVDS differential data input. Channel O1 (odd)  |
| 5   | RXO2- | Negative LVDS differential data input. Channel O2 (odd)  |
| 6   | RXO2+ | Positive LVDS differential data input. Channel O2 (odd)  |
| 7   | GND   | Ground   |
| 8   | RXOC- | Negative LVDS differential clock input. (odd)            |
| 9   | RXOC+ | Positive LVDS differential clock input. (odd)            |
| 10  | RXO3- | Negative LVDS differential data input. Channel O3(odd)   |
| 11  | RXO3+ | Positive LVDS differential data input. Channel O3 (odd)  |
| 12  | RXE0- | Negative LVDS differential data input. Channel E0 (even) |
| 13  | RXE0+ | Positive LVDS differential data input. Channel E0 (even) |
| 14  | GND   | Ground   |
| 15  | RXE1- | Negative LVDS differential data input. Channel E1 (even) |
| 16  | RXE1+ | Positive LVDS differential data input. Channel E1 (even) |
| 17  | GND   | Ground   |
| 18  | RXE2- | Negative LVDS differential data input. Channel E2 (even) |
| 19  | RXE2+ | Positive LVDS differential data input. Channel E2 (even) |
| 20  | RXEC- | Negative LVDS differential clock input. (even)           |
| 21  | RXEC+ | Positive LVDS differential clock input. (even)           |
| 22  | RXE3- | Negative LVDS differential data input. Channel E3 (even) |
| 23  | RXE3+ | Positive LVDS differential data input. Channel E3 (even) |

|    |     |   |
|----|-----|---|
| 24 | GND | Ground                                    |
| 25 | NC  | For LCD internal use only, Do not connect |
| 26 | NC  | For LCD internal use only, Do not connect |
| 27 | NC  | For LCD internal use only, Do not connect |
| 28 | Vcc | +5.0V power supply                        |
| 29 | Vcc | +5.0V power supply                        |
| 30 | Vcc | +5.0V power supply                        |

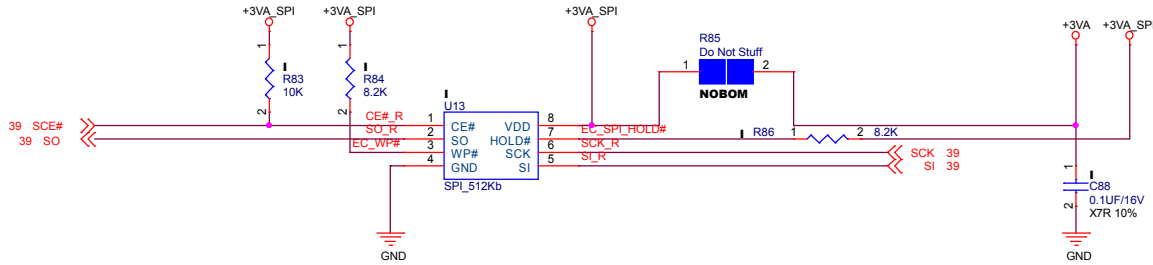




|              |        |       |              |
|--------------|--------|-------|--------------|
| BL_EN        | NOBOM1 | OPT3  | Do Not Stuff |
| SMB_CLK_ANX  | NOBOM1 | OPT4  | Do Not Stuff |
| SMB_DATA_ANX | NOBOM1 | OPT5  | Do Not Stuff |
| BLKT_CTRL    | NOBOM1 | OPT6  | Do Not Stuff |
| GND          | NOBOM1 | OPT7  | Do Not Stuff |
| VLED_CVB     | NOBOM1 | OPT8  | Do Not Stuff |
| ILED1_CVB    | NOBOM1 | OPT10 | Do Not Stuff |
| ILED2_CVB    | NOBOM1 | OPT11 | Do Not Stuff |
| ILED3_CVB    | NOBOM1 | OPT12 | Do Not Stuff |
| ILED4_CVB    | NOBOM1 | OPT13 | Do Not Stuff |
| PNL_ID0      | NOBOM1 | OPT14 | Do Not Stuff |
| GND          | NOBOM1 | OPT18 | Do Not Stuff |
| GND          | NOBOM1 | OPT19 | Do Not Stuff |
| GND          | NOBOM1 | OPT20 | Do Not Stuff |
| GND          | NOBOM1 | OPT21 | Do Not Stuff |
| GND          | NOBOM1 | OPT22 | Do Not Stuff |



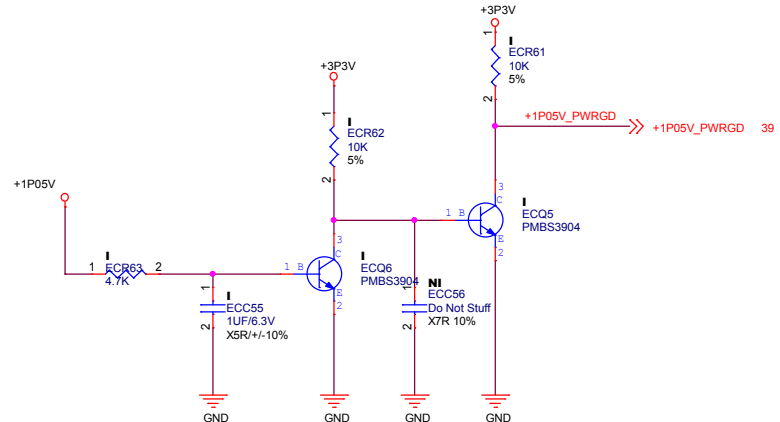
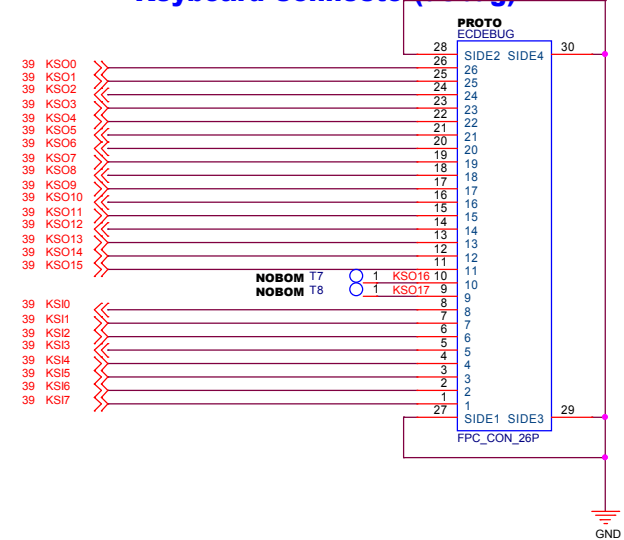
**SPI ROM+**  
**External programming conn.**



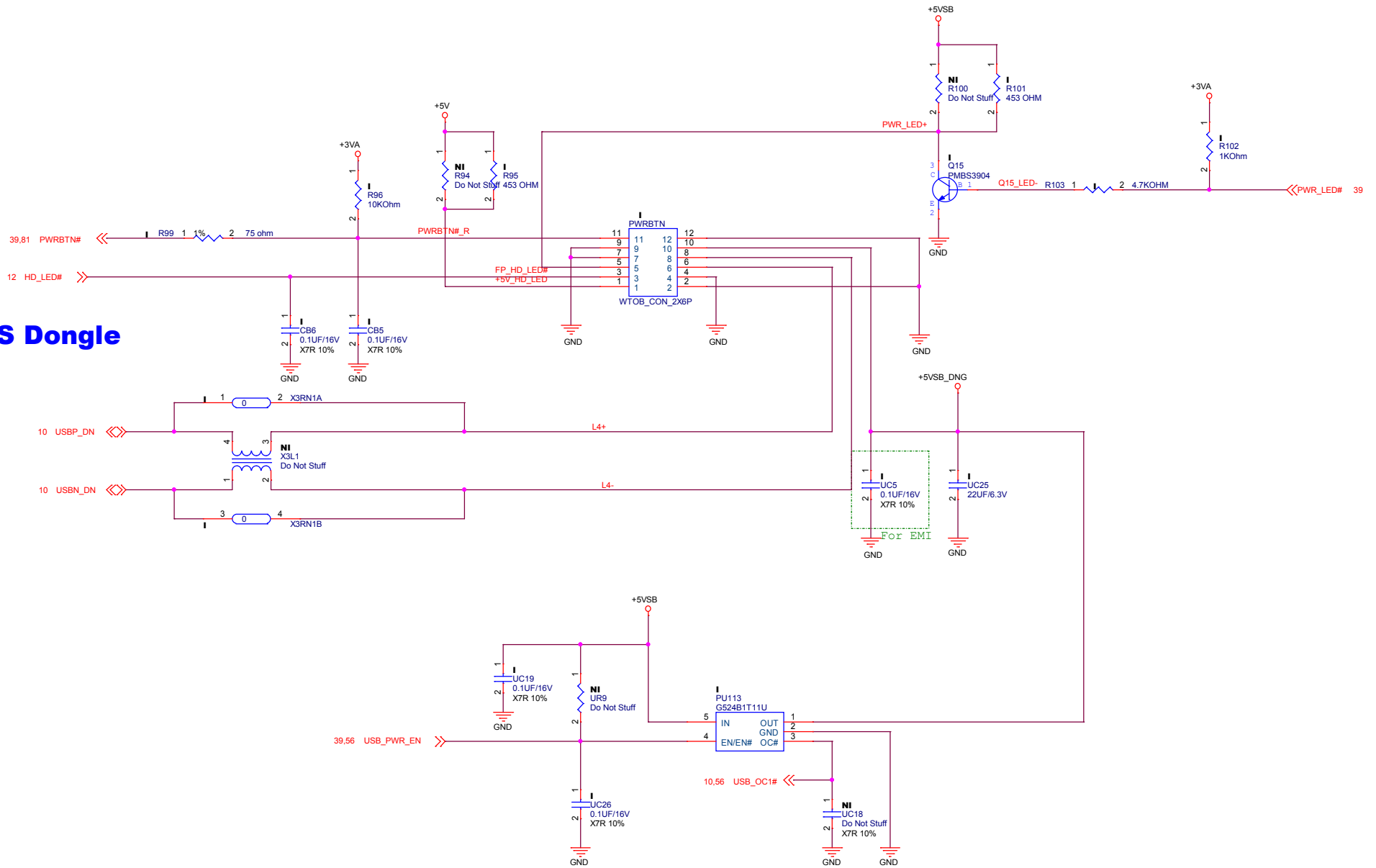
### For EC PU/PD



## Keyboard Connector(debug)

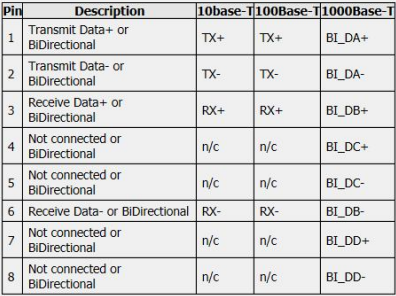


# KB/MS Dongle

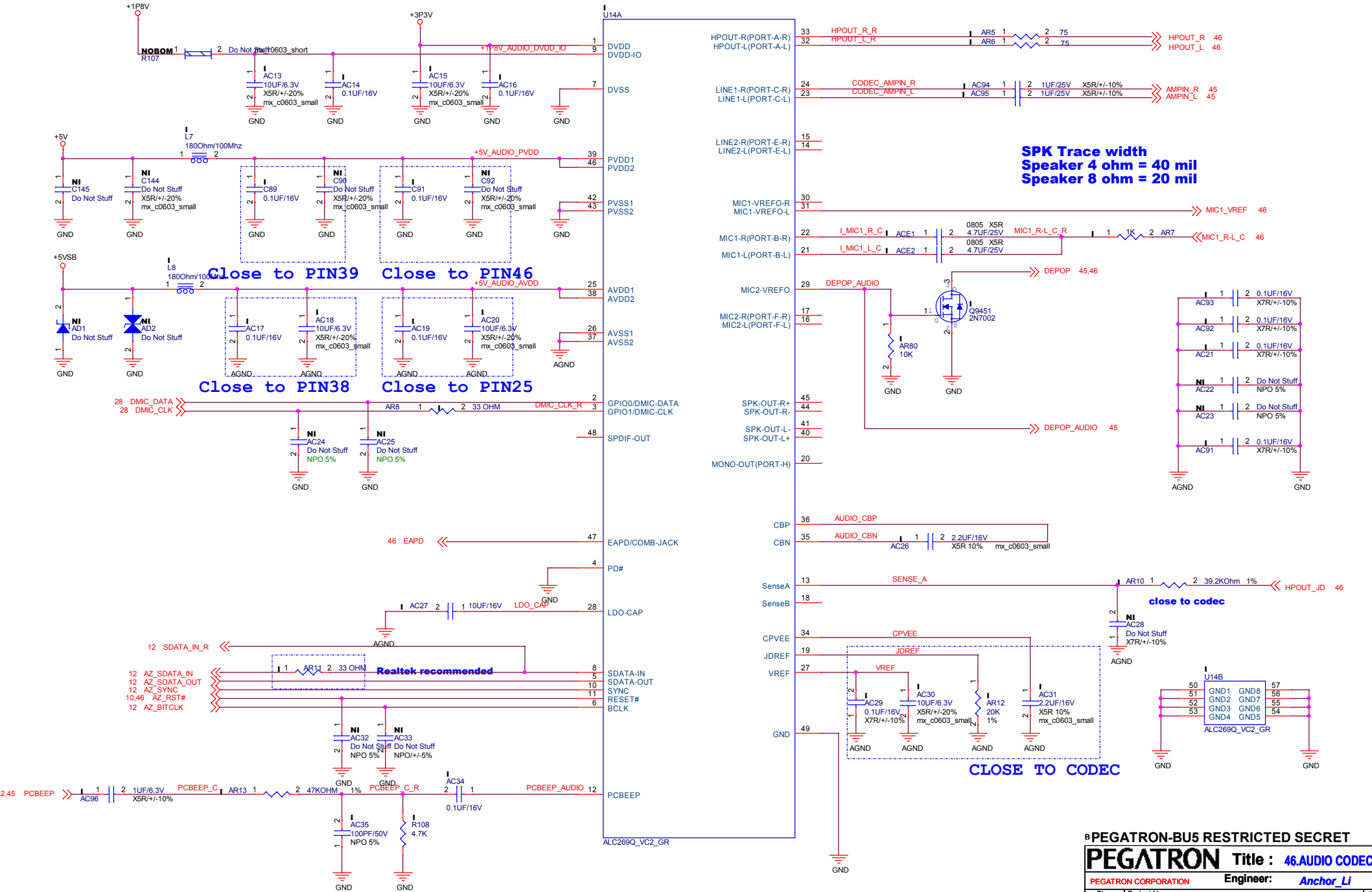


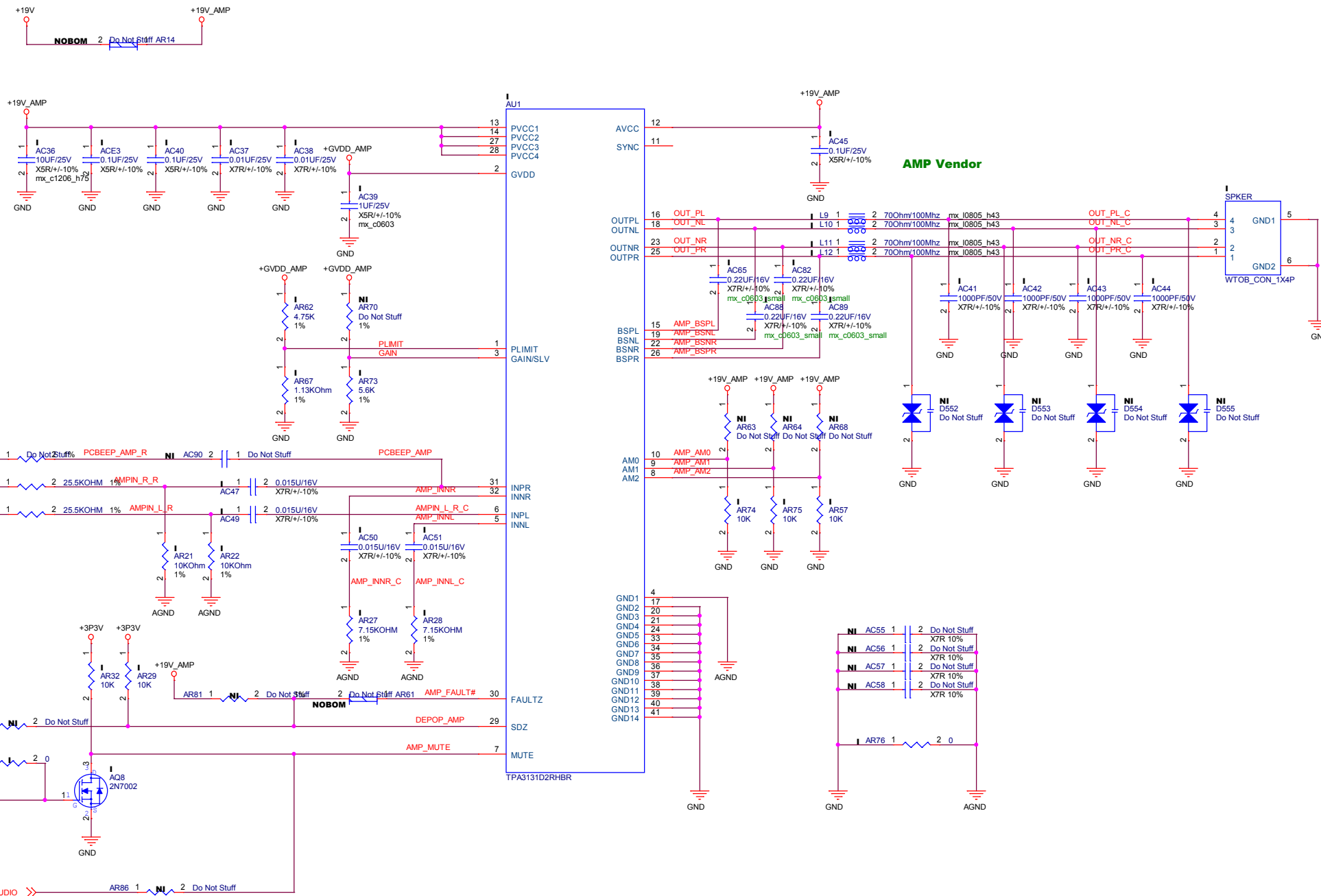




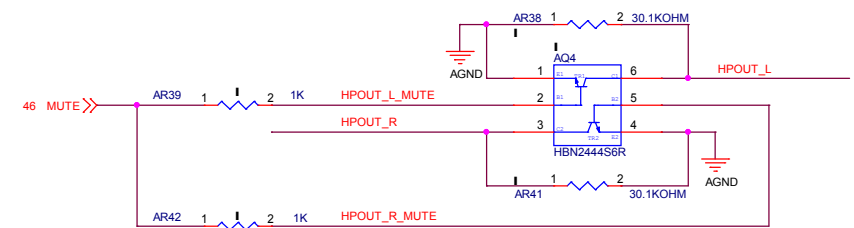
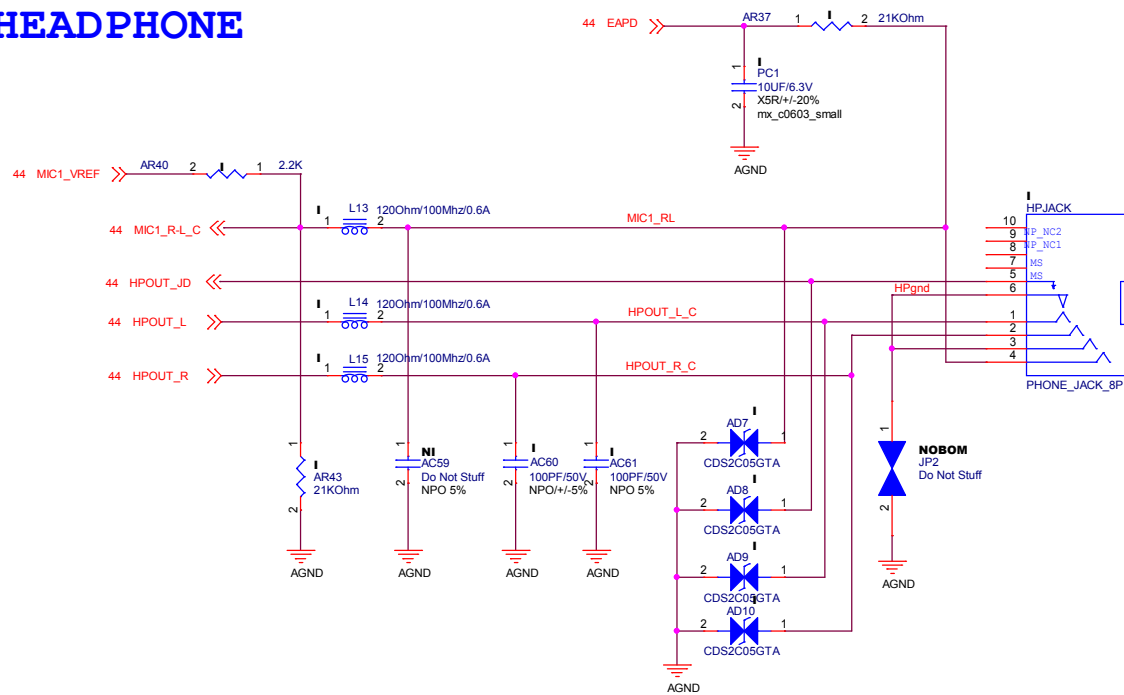


ALC269 CODEC

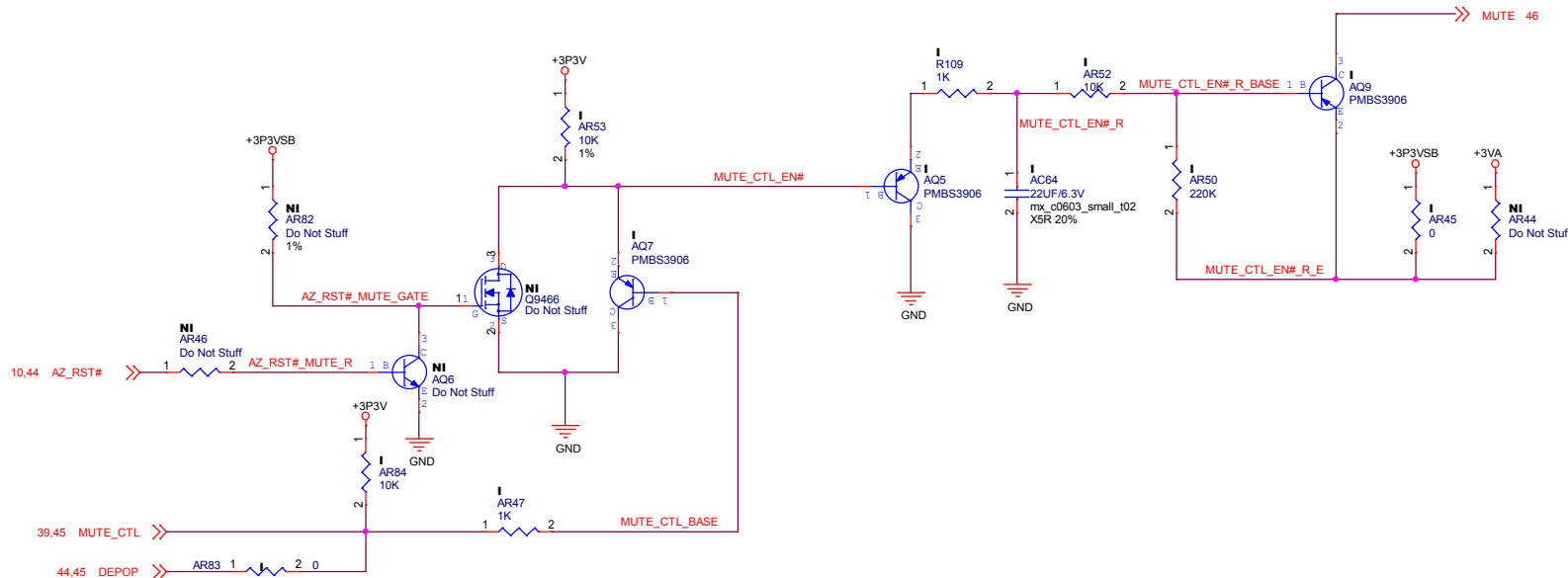




## HEADPHONE



**Audio MUTE**



|                                    |                                  |   |              |
|------------------------------------|----------------------------------|---|--------------|
| 5 PEGATRON DT-MB RESTRICTED SECRET |                                  |   |              |
| <b>PEGATRON</b>                    |                                  | <b>Title :</b> 48.REAR LINE OUT& GHS CONN |              |
| PEGATRON CORPORATION               |                                  | <b>Engineer:</b> <u>Anchor_Li</u>         |              |
| Size<br>A3                         | Project Name<br><b>IPMAL-BR3</b> |   | Rev<br>R1.02 |
| Date: Monday, September 05, 2016   | Sheet                            | 46  | of 81        |

PCB1  
PCB BOARD

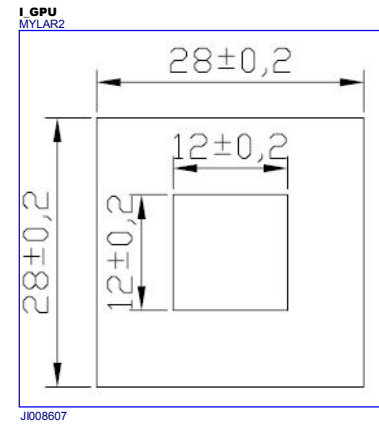
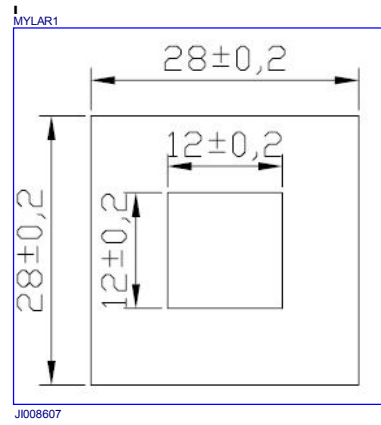
IPMBW-BR  
PCB  
Proprietary

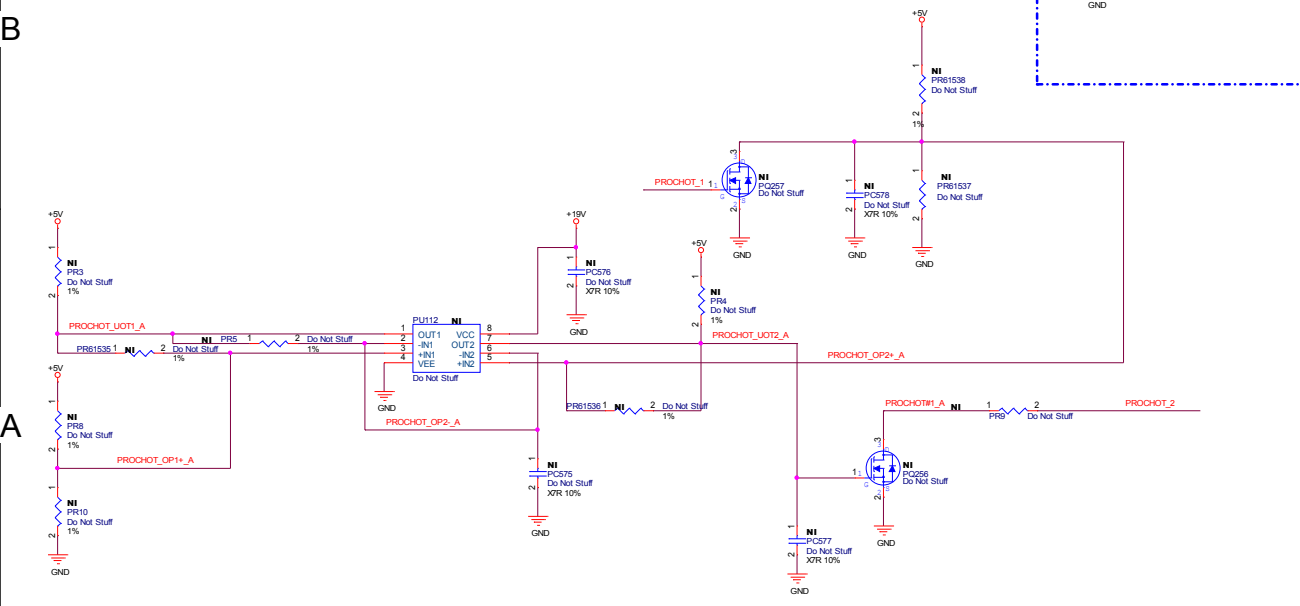
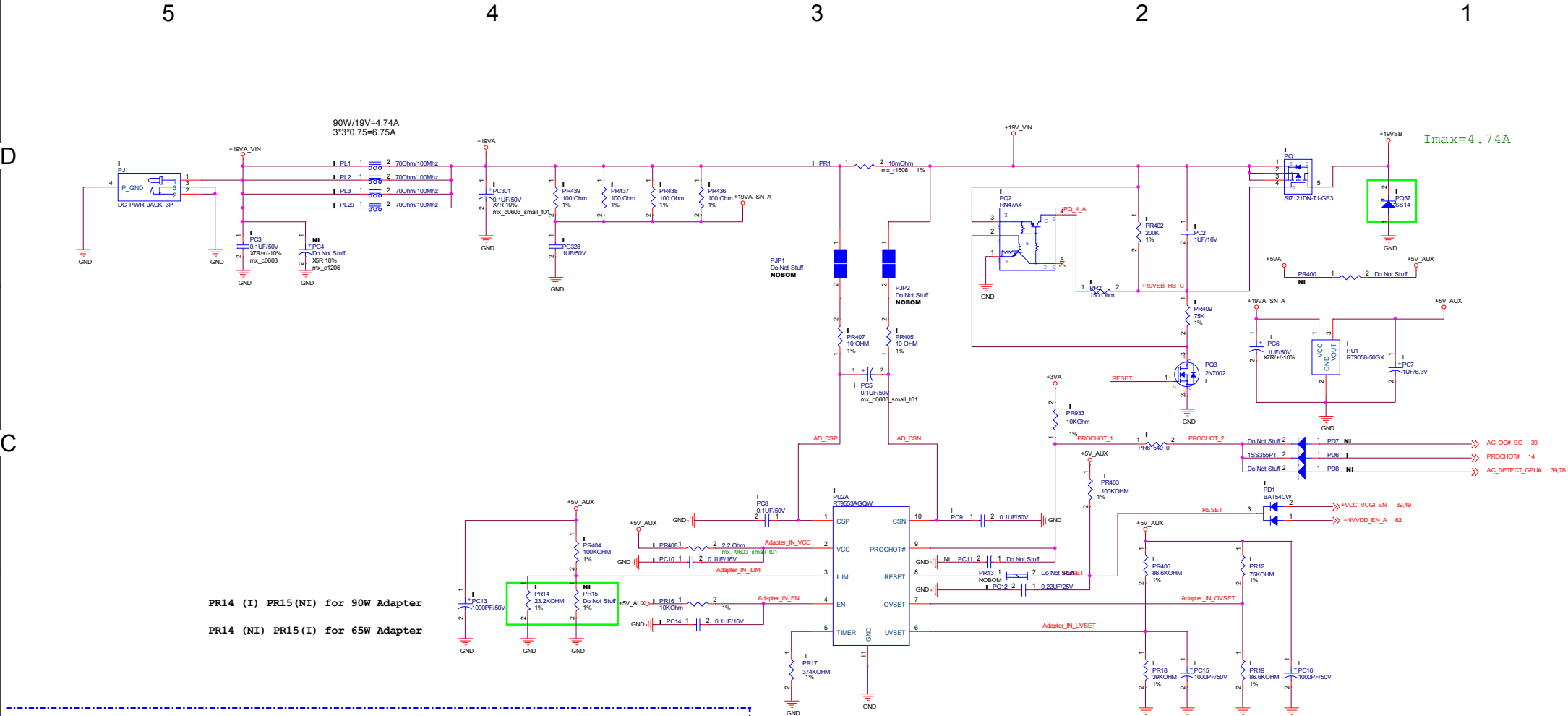
SN\_LABEL  
42X7\_WHITE

IMP  
AMILB  
PCB  
AMI label

BPLATE  
BACK PLATE

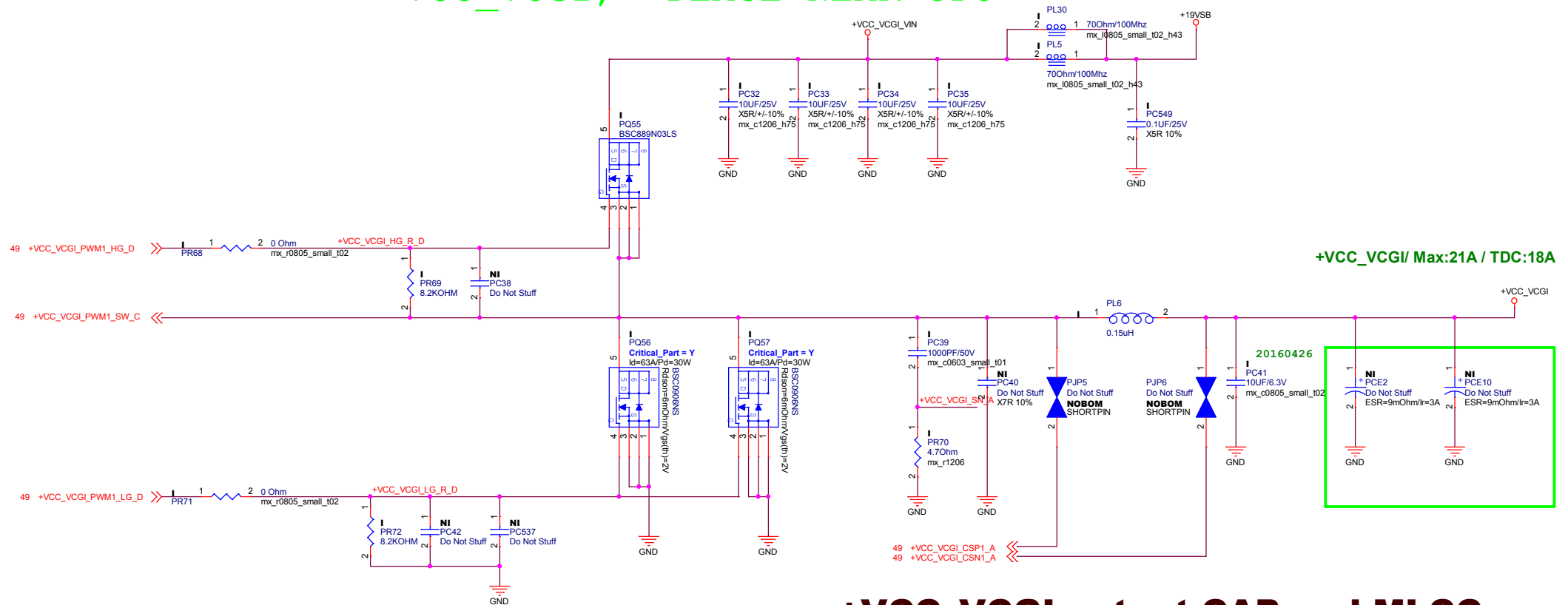
IPMBW-BR  
BACK PLATE





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+VCC\_VCGI, PLACE NEAR CPU



## +VCC\_VCGI output CAP and MLCC

**220uF \* 2 pcs**  
**22uF \* 22pcs**

| Owner  | VCC_VCGI OCP | Low limit | High limit     |
|--------|--------------|-----------|----------------|
| Adam   | 33.6A@25deg  | 21A       | 45A@0.15uH-20% |
| Renton | 33.6A@25deg  | 21A       | 45A@0.15uH-20% |

|        |         |  |      |               |         |
|--------|---------|--|------|---------------|---------|
|        |         | $V_{SET2} = V_{REF} \times \frac{R2}{R1 + R2}$ |      | TONSET (kTON) | CCS (%) |
| Min    | Typical | Max  | Unit |               |         |
| 3.75   | 25      | 46.25  | mV   | 15            | 120     |
| 54.25  | 75      | 95.75  | mV   |               | 140     |
| 104.75 | 125     | 145.25   | mV   |               | 160     |
| 155.25 | 175     | 194.75   | mV   |               | 180     |
| 205.75 | 225     | 244.25   | mV   |               | 120     |
| 256.25 | 275     | 293.75   | mV   | 13            | 140     |
| 306.75 | 325     | 343.25   | mV   |               | 160     |

|                                  |                                  |  |       |
|----------------------------------|----------------------------------|--|-------|
| <b>PEGATRON</b>                  |                                  | <b>Title :</b> 53.+VCC_VCGI DRIVER & CAP |       |
| <b>PEGATRON CORPORATION</b>      |                                  | <b>Engineer:</b> Anchor_Li               |       |
| Size<br><b>A3</b>                | Project Name<br><b>IPMAL-BR3</b> | Rev<br><b>R1.02</b>                      |       |
| Date: Monday, September 05, 2016 | Sheet                            | 50                                       | of 81 |

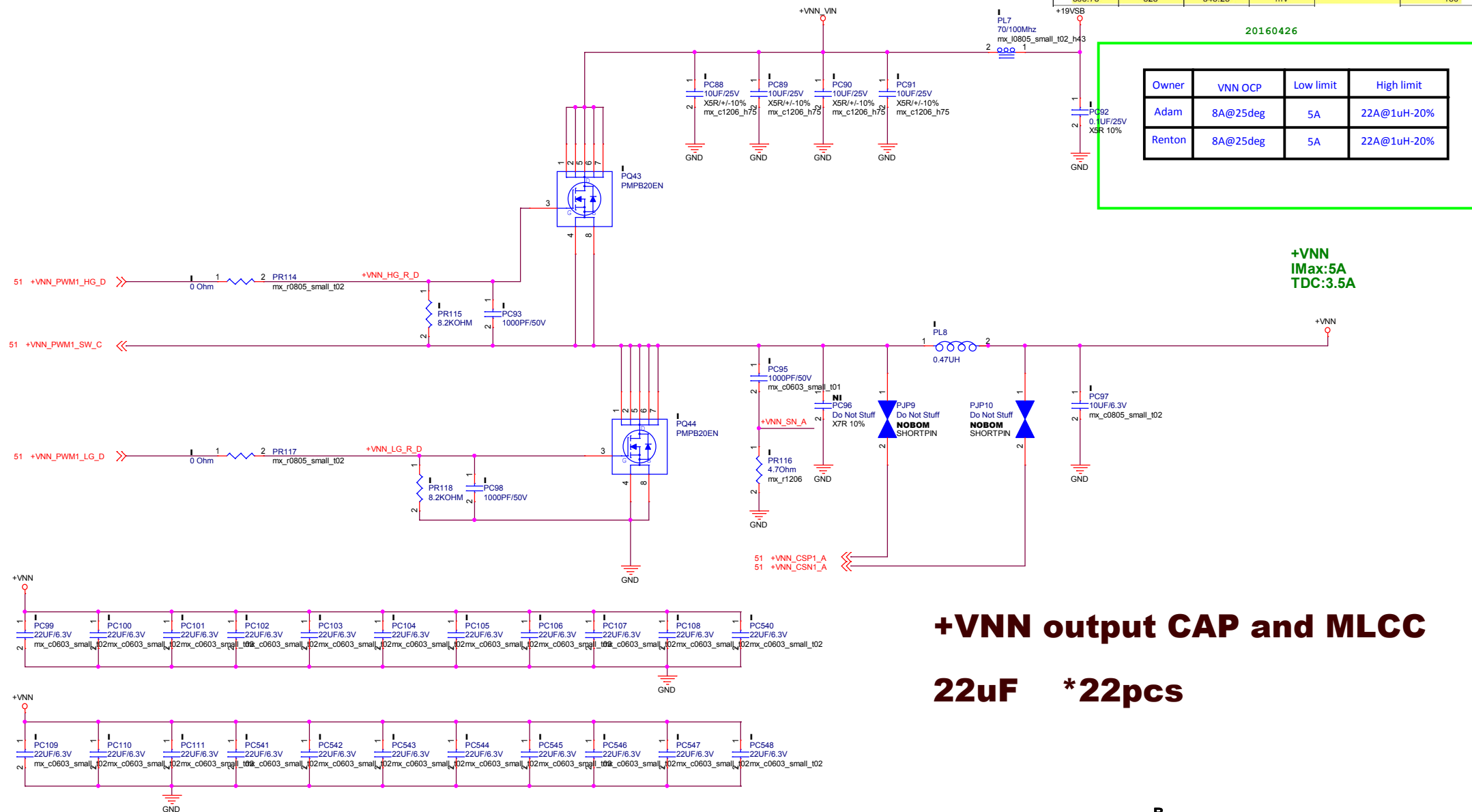




+VNN, PLACE NEAR CPU

$$V_{SET2} = V_{REF} \times \frac{R2}{R1+R2}$$

| Min    | Typical | Max    | Unit | TONSET (KTON) | OCS (%) |
|--------|---------|--------|------|---------------|---------|
| 3.75   | 25      | 46.25  | mV   | 15            | 120     |
| 54.25  | 75      | 95.75  | mV   |               | 140     |
| 104.75 | 125     | 145.25 | mV   |               | 160     |
| 155.25 | 175     | 194.75 | mV   |               | 180     |
| 205.75 | 225     | 244.25 | mV   |               | 120     |
| 256.25 | 275     | 293.75 | mV   | 13            | 140     |
| 306.75 | 325     | 343.25 | mV   |               | 160     |



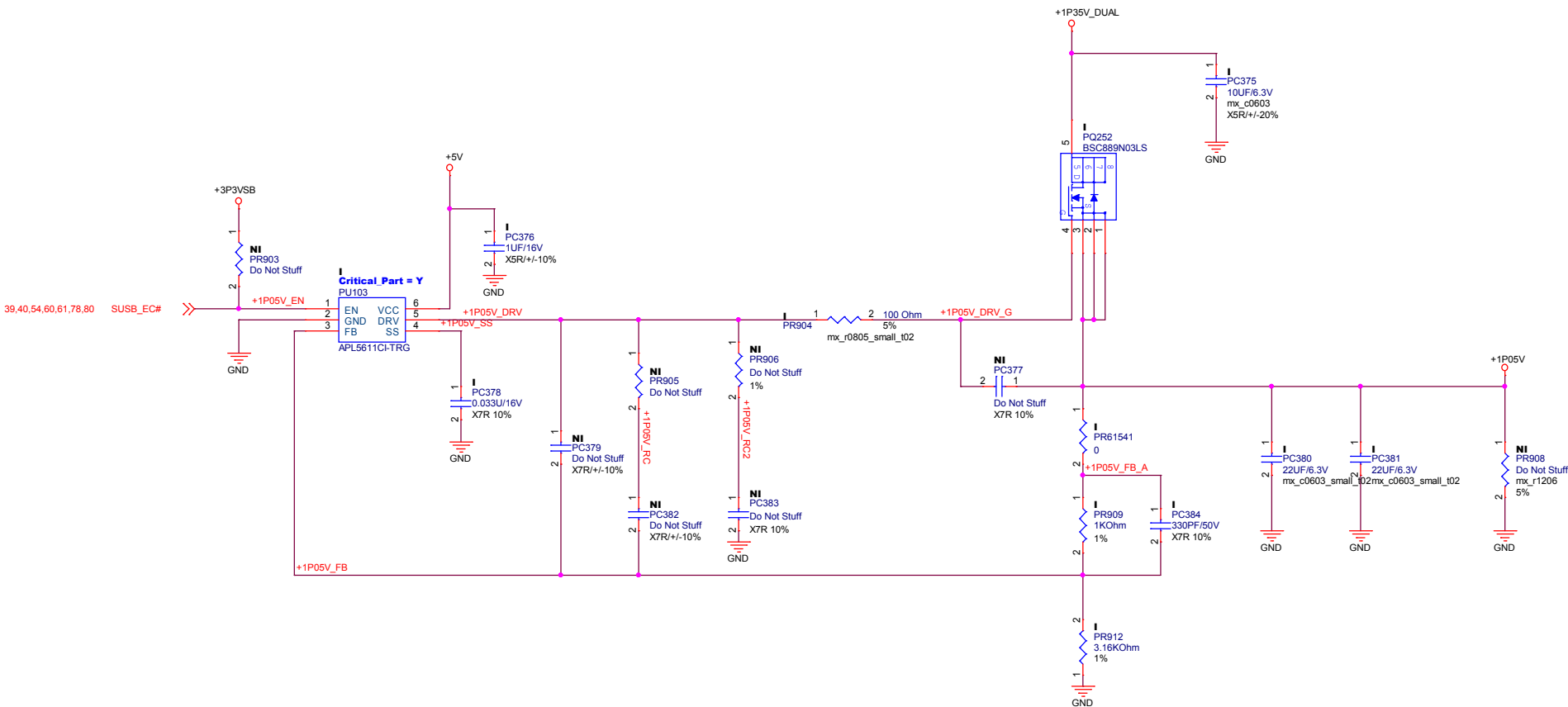
20160426

| Owner  | VNN OCP  | Low limit | High limit  |
|--------|----------|-----------|-------------|
| Adam   | 8A@25deg | 5A        | 22A@1uH-20% |
| Renton | 8A@25deg | 5A        | 22A@1uH-20% |

+VNN  
IMax:5A  
TDC:3.5A

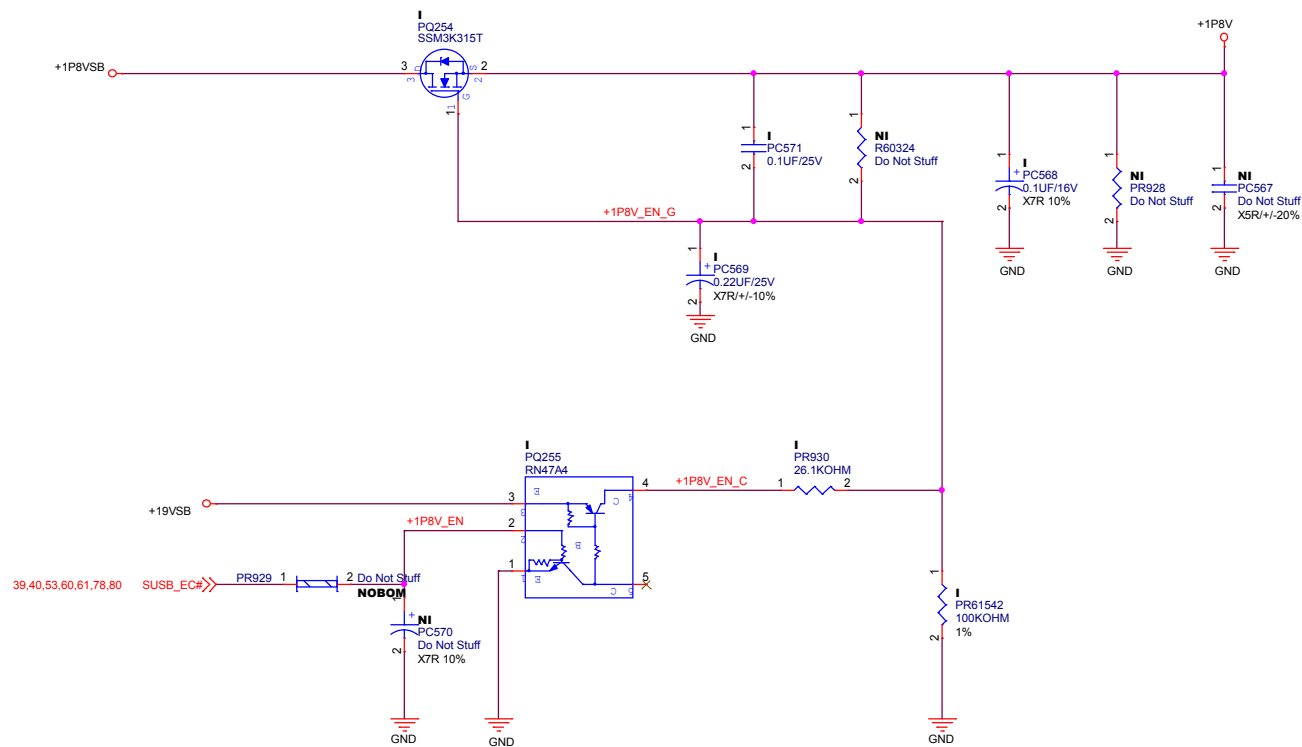
+VNN output CAP and MLCC

22uF \*22pcs

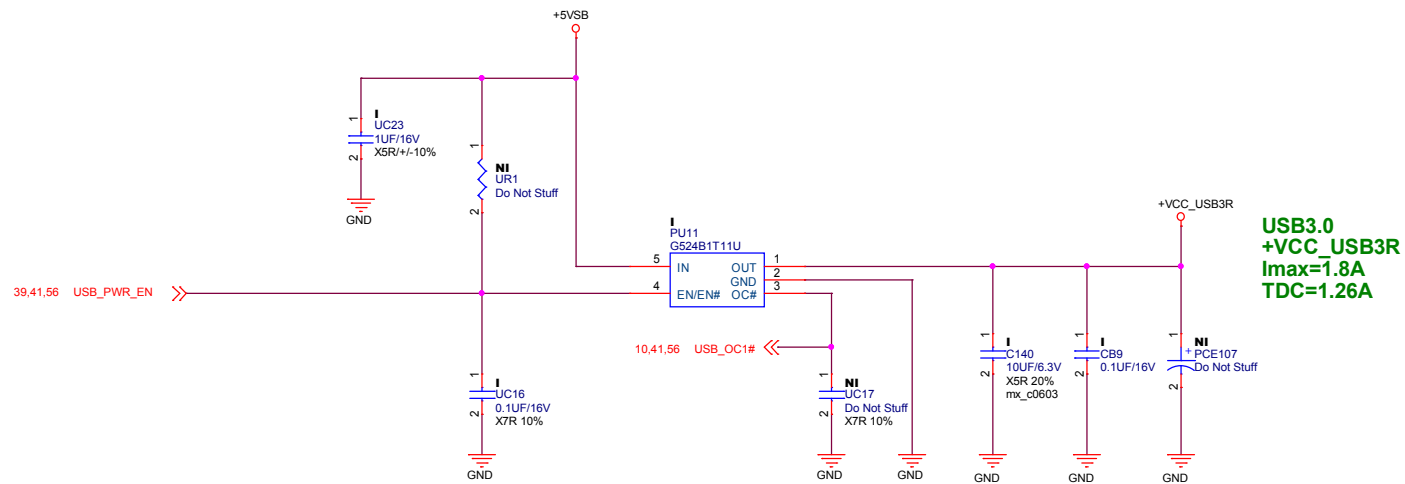
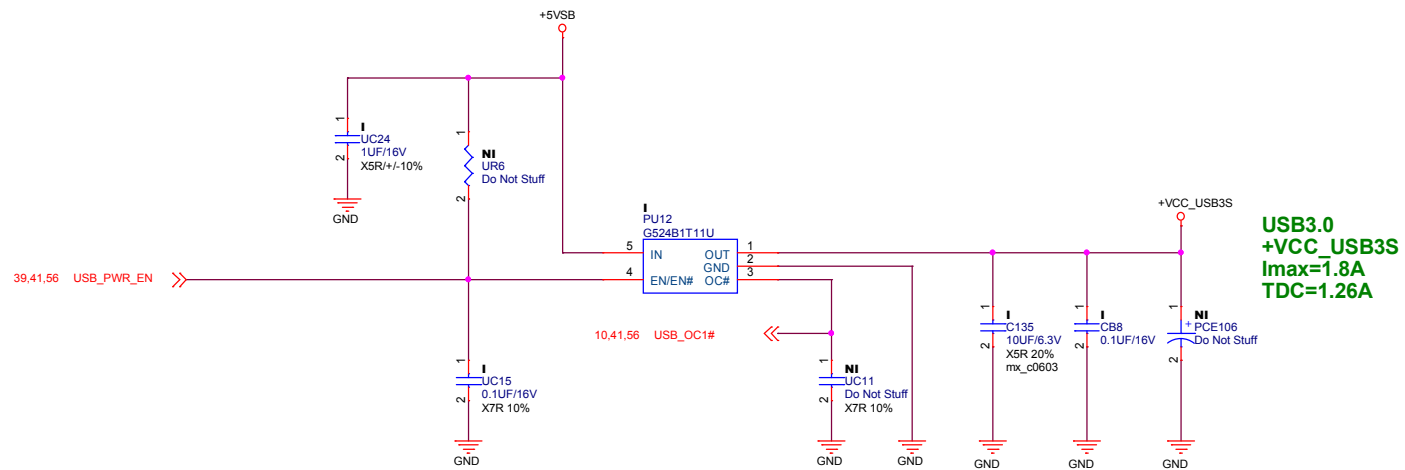


B

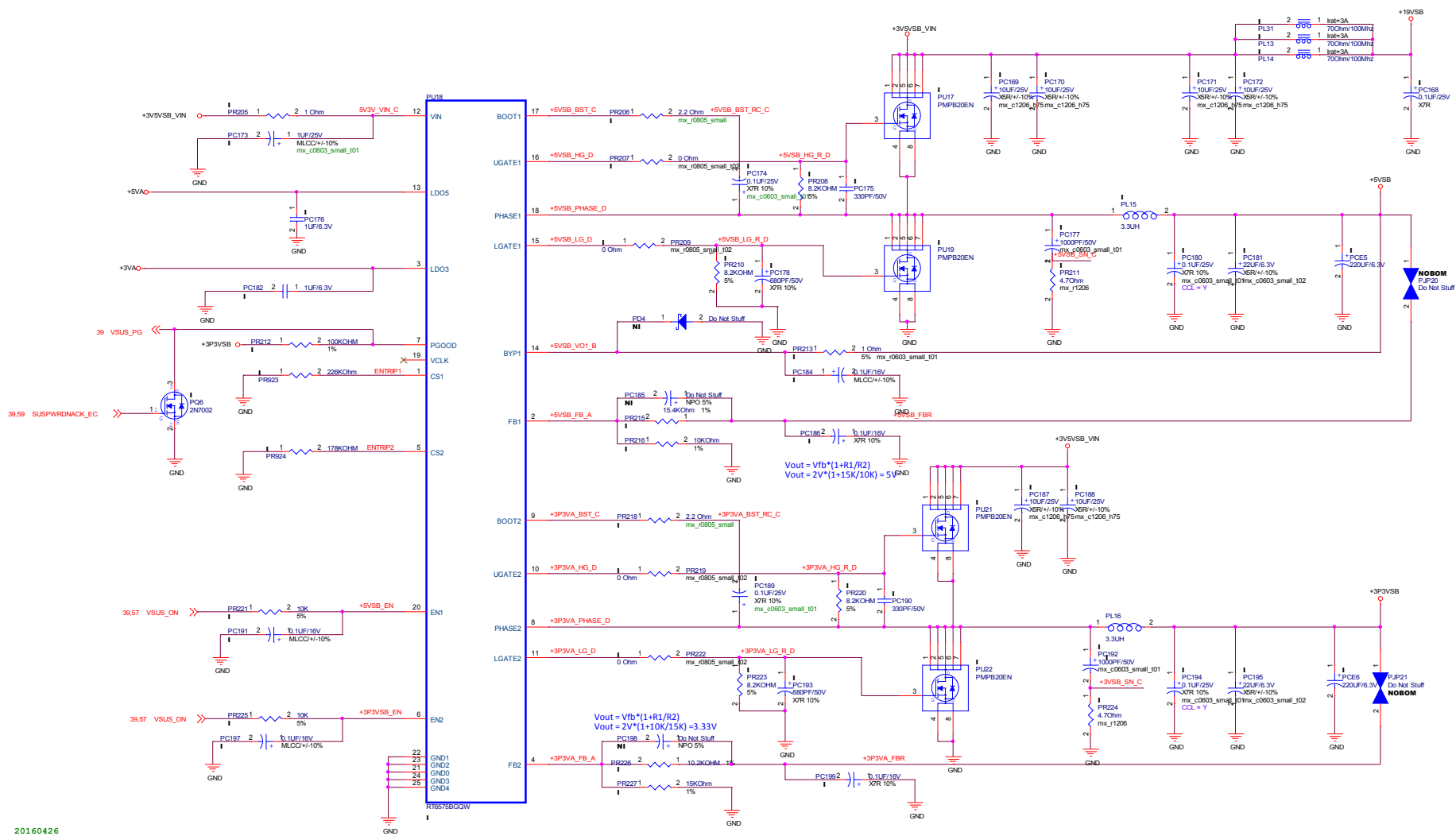
|                                  |                           |                     |             |
|----------------------------------|---------------------------|---------------------|-------------|
| PEGATRON                         |                           | Title : 56.1P05V    |             |
| PEGATRON CORPORATION             |                           | Engineer: Anchor_Li |             |
| Size<br>A3                       | Project Name<br>IPMAL-BR3 |                     | Rev<br>R1.0 |
| Date: Monday, September 05, 2016 |                           | Sheet 53 of 81      |             |







$$I_{in}=2.68A+1.407A=4.087A$$



20160426

**+5VSB**  
I<sub>max</sub>=8.15A  
TDC=5.705A

F<sub>sw</sub>=300KHz  
I<sub>in</sub>=2.68A  
I<sub>ripple</sub>=3.72A  
I<sub>ripple</sub>=33.49mV  
OCP=13.78A

20160426

**+3P3VSB**  
I<sub>max</sub>=6.48A  
TDC=4.536A

F<sub>sw</sub>=355KHz  
I<sub>in</sub>=1.407A  
I<sub>ripple</sub>=2.33A  
I<sub>ripple</sub>=20.95mV  
OCP=11.09A

20160426

RDS(ON)=28.7mohm(worse case)/20.5mohm(25deg)-PMP8202EN

| Owner  | +5VSB OCP point             | Low limit | High limit    |
|--------|-----------------------------|-----------|---------------|
| Adam   | 13.78A@25deg<br>9.84A@worse | 8.15A     | 14A@3.3uH-24% |
| Renton | 13.78A@25deg<br>9.84A@worse | 8.15A     | 14A@3.3uH-24% |

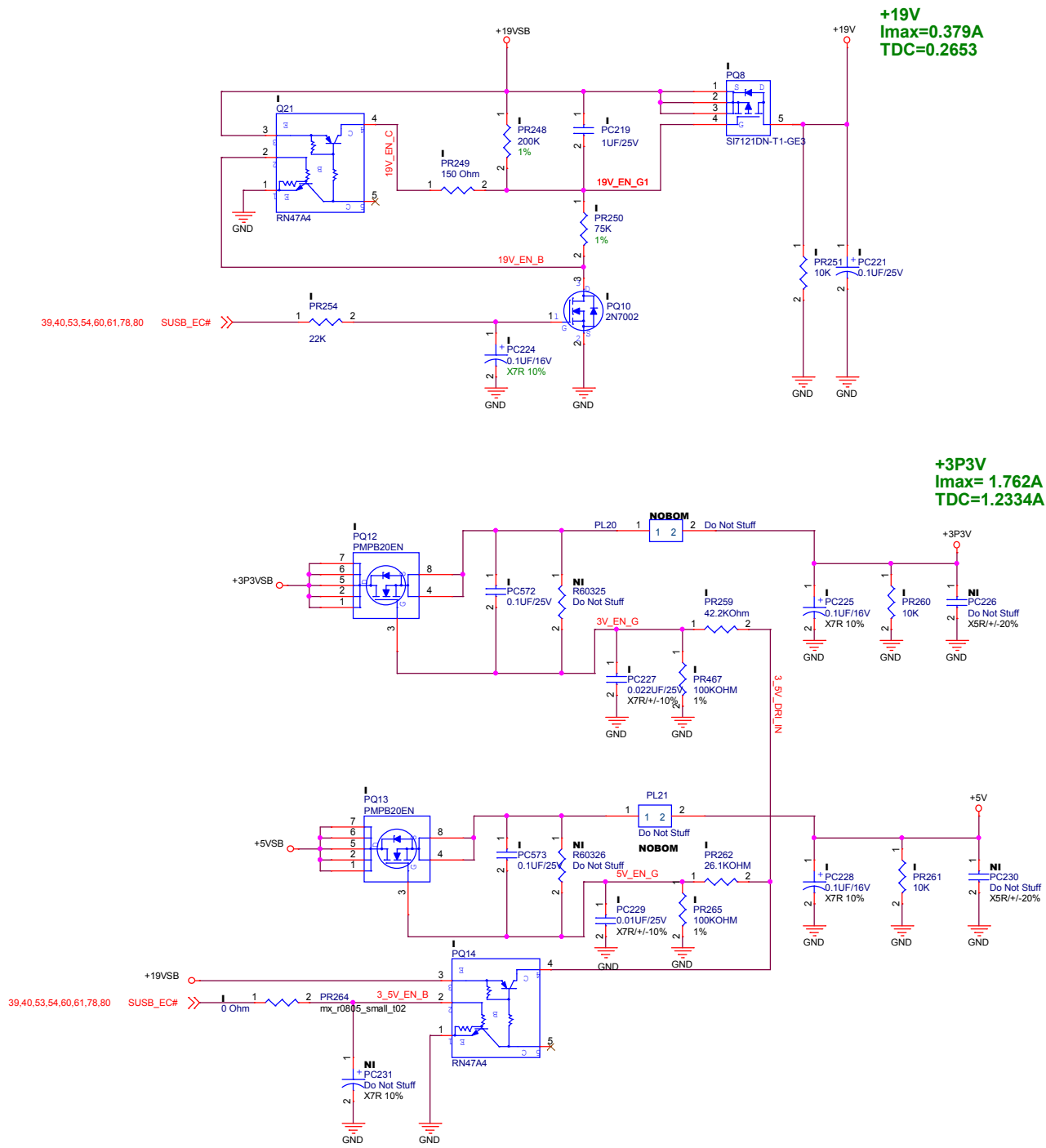
| Owner  | 3P3VSB OCP point            | Low limit | High limit      |
|--------|-----------------------------|-----------|-----------------|
| Adam   | 11.09A@25deg<br>7.92A@worse | 6.48A     | 13.5A@3.3uH-20% |
| Renton | 11.09A@25deg<br>7.92A@worse | 6.48A     | 13.5A@3.3uH-20% |

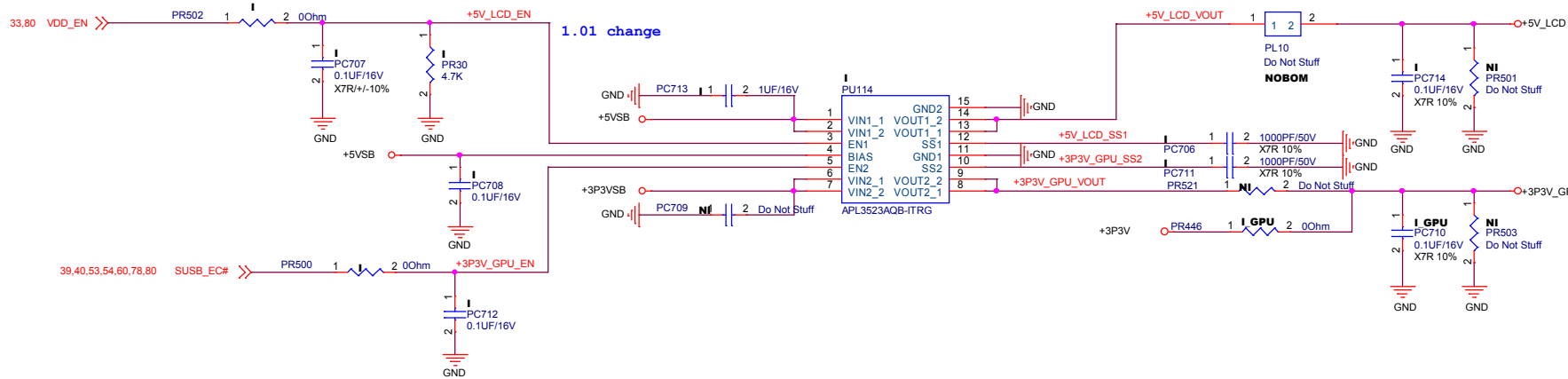
RLIMIT = ( I LIMIT \* RDS(ON) ) \* 8 / 10uA











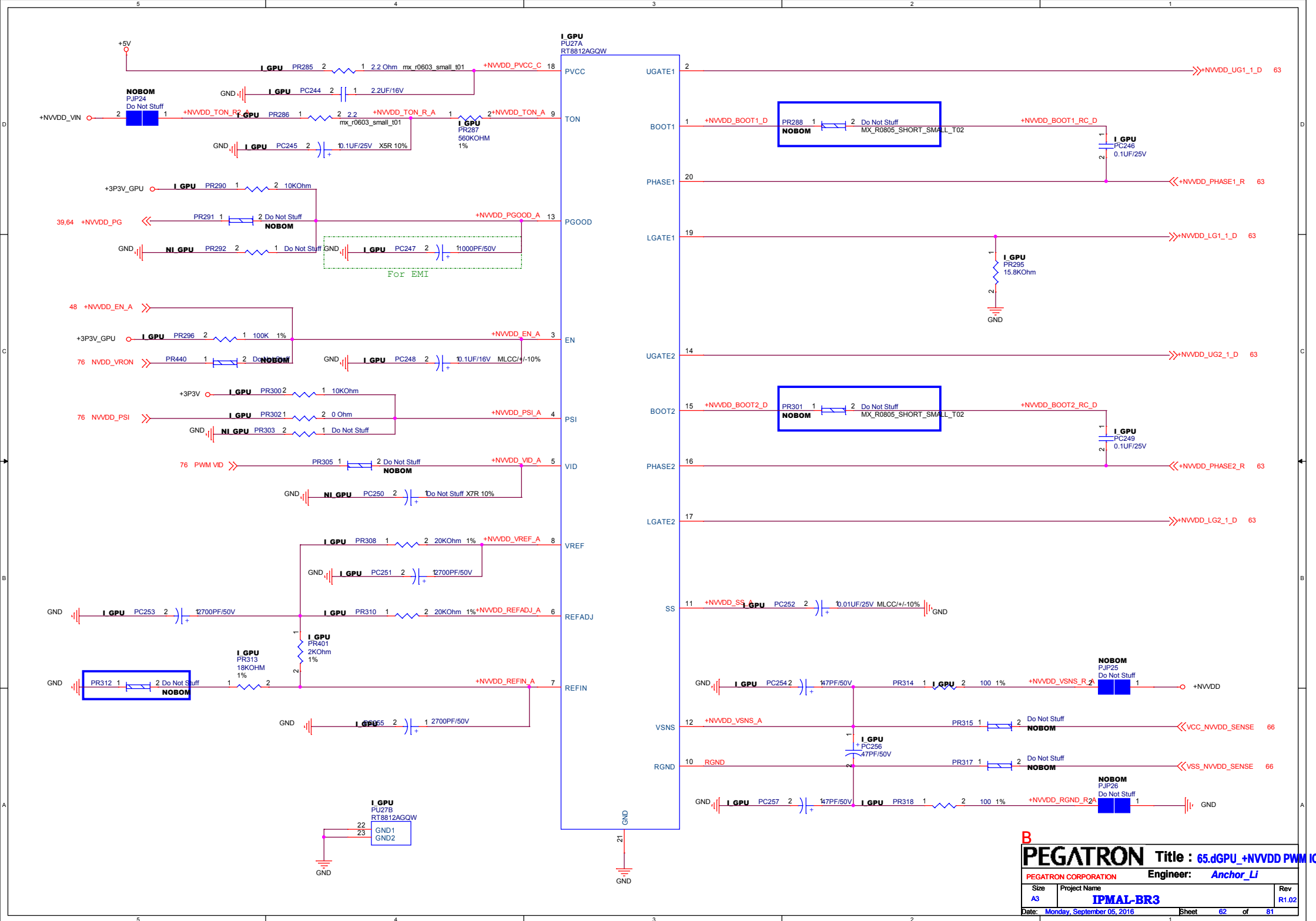
**+5VSB ==> +5V\_LCD**  
**I<sub>max</sub>=1.65A**

R<sub>ds(on)</sub>=25m ohm  
 I<sub>d</sub>=0.112A  
 P<sub>d</sub>=0.112^2\*25m=0.31mW  
 V<sub>drop</sub>=0.16\*25m=4mV

**+3P3V\_GPU**  
**I<sub>max</sub>=0.342A**  
**Trace Width>50mil**

**B**

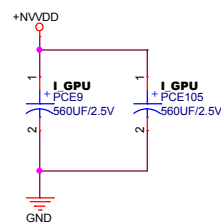
| PEGATRON                         |              |       | Title : 64.5V_LCD          |       |
|----------------------------------|--------------|-------|----------------------------|-------|
| PEGATRON CORPORATION             |              |       | Engineer: <u>Anchor_Li</u> |       |
| Size                             | Project Name |       |                            | Rev   |
| A3                               | IPMAL-BR3    |       |                            | R1.02 |
| Date: Monday, September 05, 2016 |              | Sheet | 61                         | of 81 |



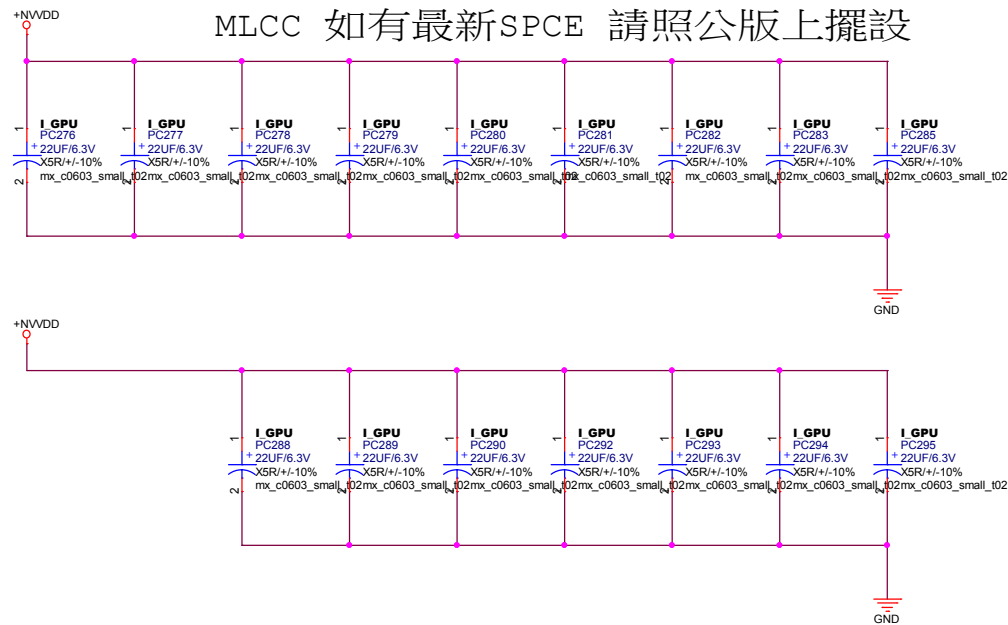




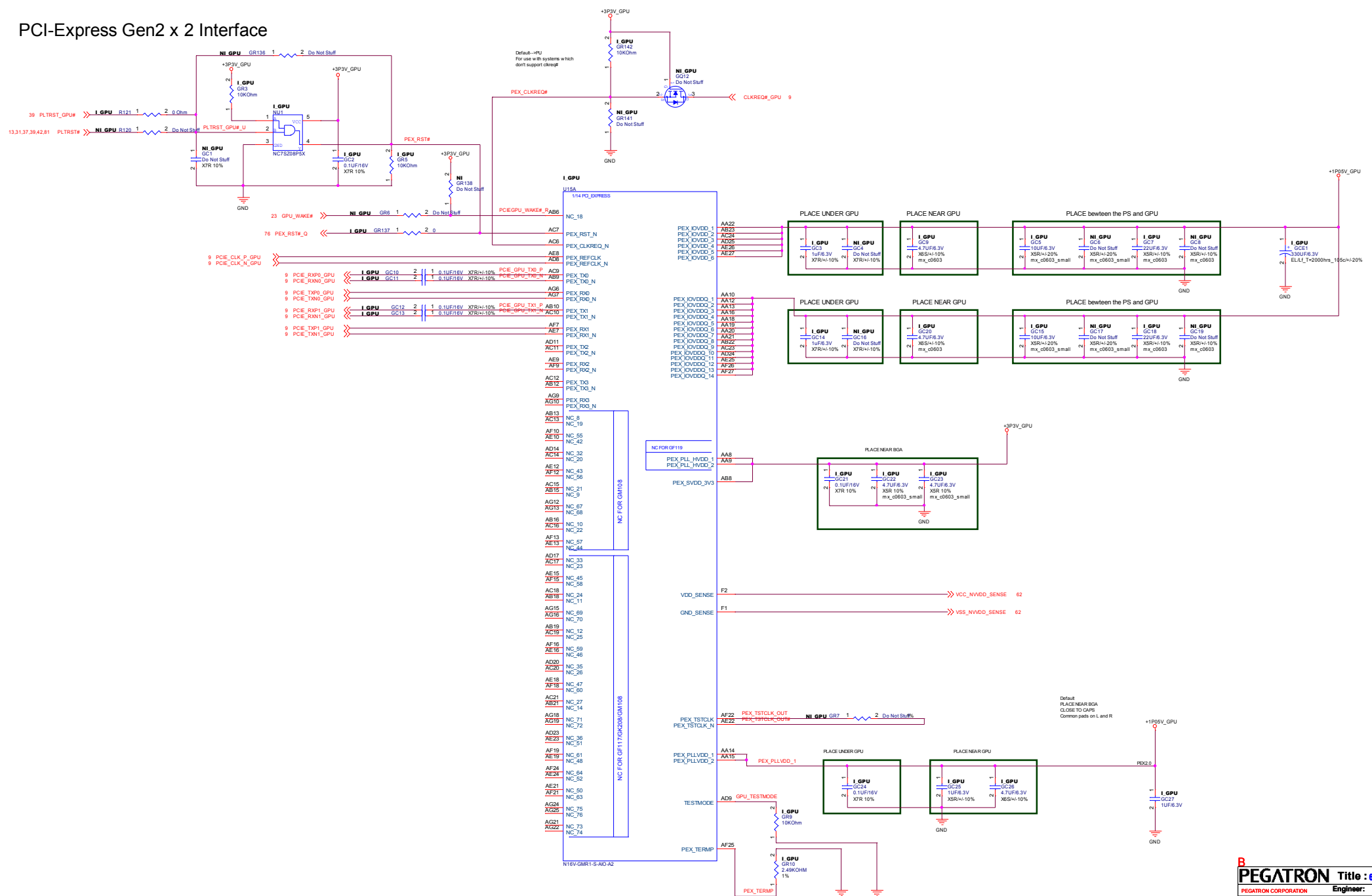
Power VR 輸出端



MLCC 如有最新SPCE 請照公版上擺設

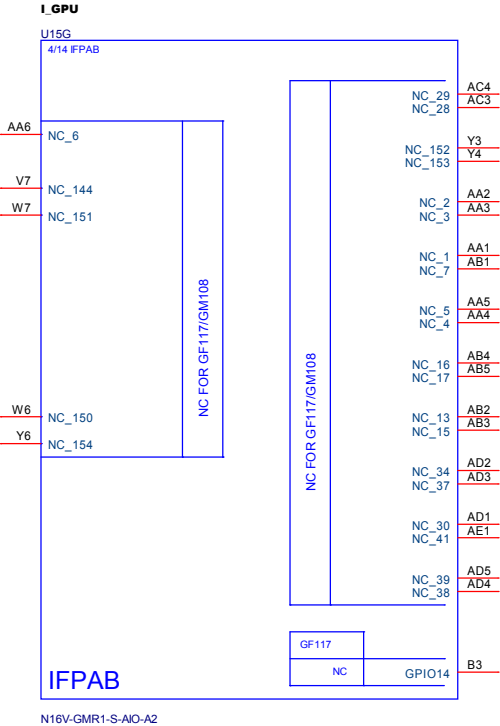


PCI-Express Gen2 x 2 Interface





IFPA/B LVDS Dual Link



Straps Mapping

Will need to check and follow the update in PUN

|           |   |   |   |   |    |          |               |         |                     |
|-----------|---|---|---|---|----|----------|---------------|---------|---------------------|
| N16V-GMR1 |   |   |   |   |    |          |               |         |                     |
| ROM_SCL   | 0 | 0 | 0 | 0 | PD | 4.99Kohm | 1%            |         |                     |
|           | 0 | 0 | 0 | 0 | PD | 4.99Kohm |               |         |                     |
|           | 0 | 0 | 0 | 1 | PD | 10.0Kohm |               |         |                     |
| ROM_SI    | 0 | 0 | 1 | 0 | PD | 15.0Kohm | 1%-001 latest | Samsung | K4W4G1646E-BC1A 0x1 |
|           | 0 | 1 | 0 | 0 | PD | 24.9Kohm |               | Hynix   | H5TC4G63CFR-N0C 0x2 |
|           | 0 | 1 | 0 | 1 | PD | 30.1Kohm |               |         |                     |
| ROM_SO    | 0 | 0 | 0 | 0 | PD | 4.99Kohm | 1%            |         |                     |
| STRAP0    |   |   |   |   | PU | 49.9Kohm | 1%            |         |                     |
| STRAP1    |   |   |   |   |    | reserved |               |         |                     |
| STRAP2    |   |   |   |   |    | reserved |               |         |                     |
| STRAP3    |   |   |   |   |    | reserved |               |         |                     |
| STRAP4    |   |   |   |   |    | reserved |               |         |                     |

| Strap Pin Name | Logical Strapping Bit 3   | Logical Strapping Bit 2 | Logical Strapping Bit 1 | Logical Strapping Bit 0 | Resistor Values | Pull-up to VDD33 | Pull-down to GND |
|----------------|---|-------------------------|-------------------------|-------------------------|-----------------|------------------|------------------|
| ROM_SCL        | SOR3_EXPOSED  | SOR2_EXPOSED            | SOR1_EXPOSED            | SOR0_EXPOSED            | 4.99 kΩ         | 1000             | 0000             |
|                |   |                         |                         |                         | 10.0 kΩ         | 1001             | 0001             |
| ROM_SI         | RAM_CFG[3]  | RAM_CFG[2]              | RAM_CFG[1]              | RAM_CFG[0]              | 15.0 kΩ         | 1010             | 0010             |
|                |   |                         |                         |                         | 20.0 kΩ         | 1011             | 0011             |
| ROM_SO         | DEVID_SEL   | PCIE_CFG                | SMB_ALT_ADDR            | VGA_DEVICE              | 24.9 kΩ         | 1100             | 0100             |
|                |   |                         |                         |                         | 30.1 kΩ         | 1101             | 0101             |
| STRAP0         | Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Stuff 49.9 kΩ pull-up. |                         |                         |                         | 34.8 kΩ         | 1110             | 0110             |
|                |   |                         |                         |                         | 45.3 kΩ         | 1111             | 0111             |
| STRAP1         | Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Do not stuff.          |                         |                         |                         |                 |                  |                  |
| STRAP2         |   |                         |                         |                         |                 |                  |                  |
| STRAP3         |   |                         |                         |                         |                 |                  |                  |
| STRAP4         |   |                         |                         |                         |                 |                  |                  |

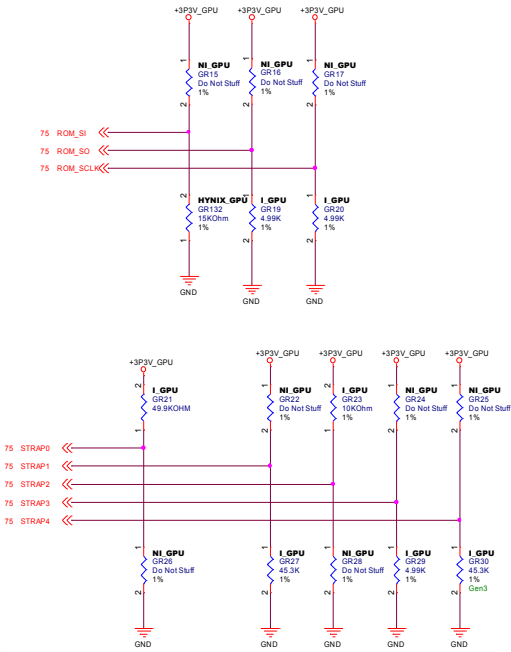
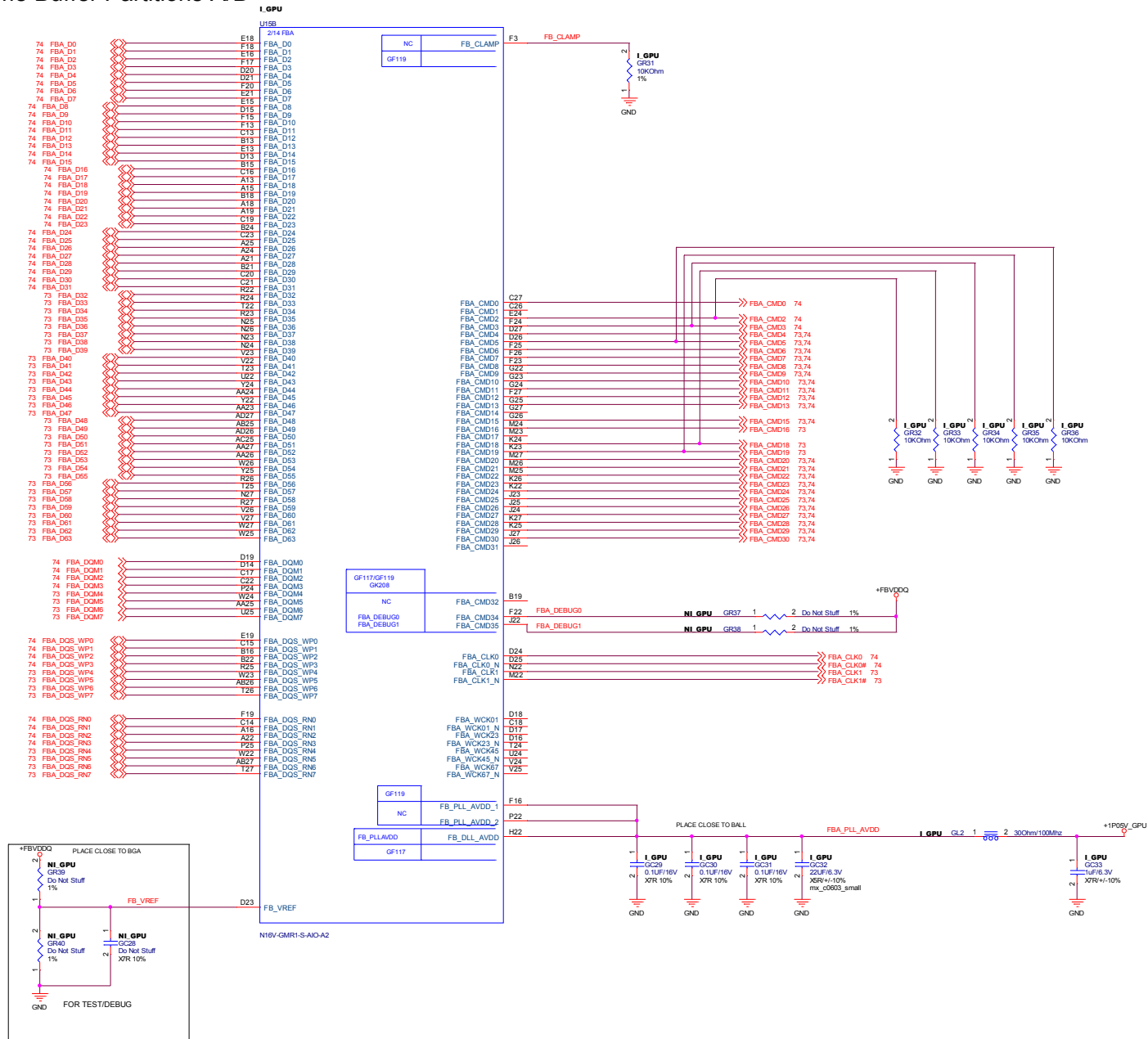


Table 13. N16V-GMR1 and N16S-GMR/-GTR DDR3 Recommended Memories

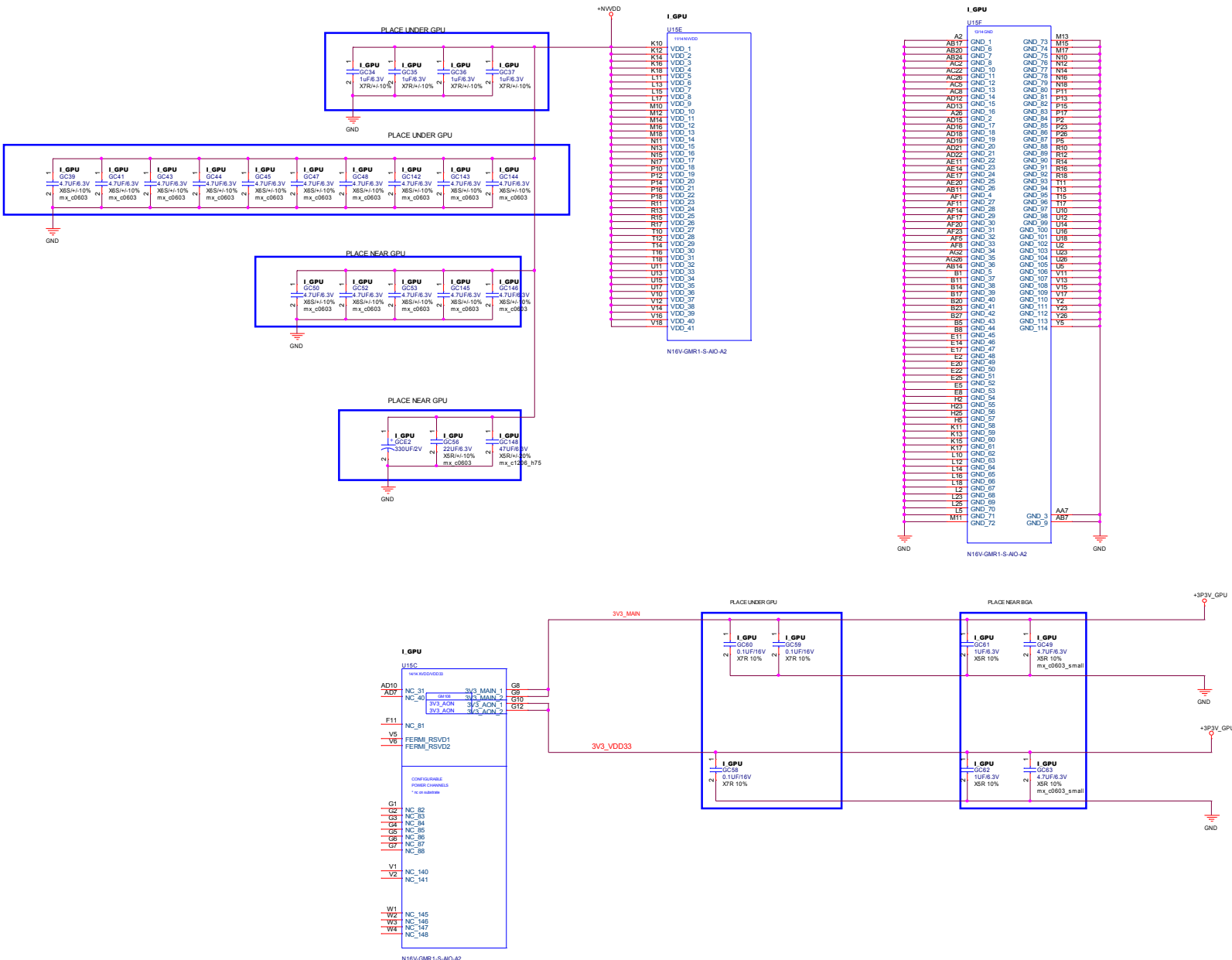
| Memory Type | FBVDD/ FBVDDQ | Memory Density | Configuration                                     | Vendor  | Manufacturer Part Number | Die Revision | Strap | Memory Speed CK Grade(MHz) | Memory Date Code Minimum | Status                    |
|-------------|---------------|----------------|---|---------|--------------------------|--------------|-------|----------------------------|--------------------------|---------------------------|
| DDR3        | 1.5V/ 1.5V    | 128Mx16        | Single Rank or Single Rank Stuffing for Dual Rank | Hynix   | H5TC2G63FFR-11C          | F-die        | 0x6   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Micron  | MT41J128M16JT-093G:K     | K-die        | 0x7   | 1000                       | 1322                     | Production ready          |
|             |               |                |   | Samsung | K4W2G1646Q-BC1A          | Q-die        | 0x8   | 1000                       | N/A                      | Production ready          |
|             |               | 256Mx16        | Single Rank or Single Rank Stuffing for Dual Rank | Hynix   | H5TC4G63AFR-11C          | A-die        | 0x0   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Micron  | MT41J256M16HA-093G:E     | E-die        | 0x1   | 1000                       | 1322                     | Production ready          |
|             |               |                |   | Samsung | K4W4G1646D-BC1A          | D-die        | 0x2   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Samsung | K4W4G1646E-BC1A          | E-die        | 0x4   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Hynix   | H5TC4G63CFR-N0C          | C-die        | 0x5   | 1000                       | N/A                      | Production ready          |
|             |               |                | Dual Rank   | Micron  | MT41J256M16LY-091G:N     | N-die        | 0x3   | 1000                       | N/A                      | Post-production candidate |
|             |               |                |   | Hynix   | H5TC4G63AFR-11C          | A-die        | 0x0   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Micron  | MT41J256M16HA-093G:E     | E-die        | 0x1   | 1000                       | 1322                     | Production ready          |
|             |               |                |   | Samsung | K4W4G1646D-BC1A          | D-die        | 0x2   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Samsung | K4W4G1646E-BC1A          | E-die        | 0xD   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Hynix   | H5TC4G63CFR-N0C          | C-die        | 0xC   | 1000                       | N/A                      | Production ready          |
|             |               |                |   | Micron  | MT41J256M16LY-091G:N     | N-die        | 0x7   | 1000                       | N/A                      | Post-production candidate |

Note: For N16V-GMR1 and N16S-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

## Frame Buffer Partitions A/B



### Power/Decoupling: +NVVDD,3V3\_NV,GRND,and Optional

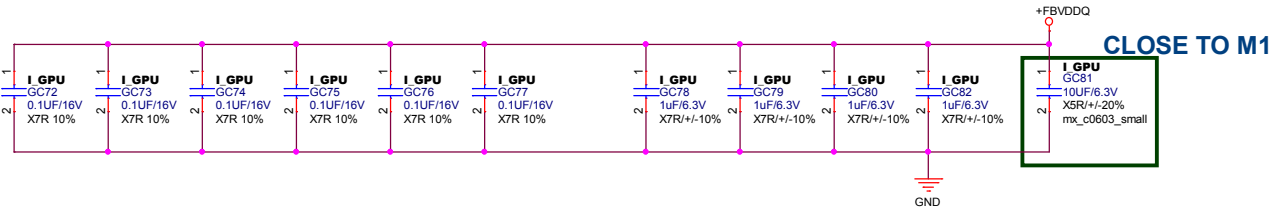


## 3

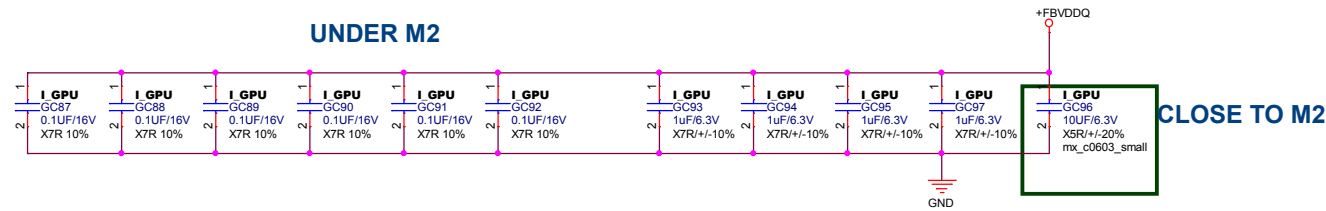


Memory FBVDD/Q Decoupling

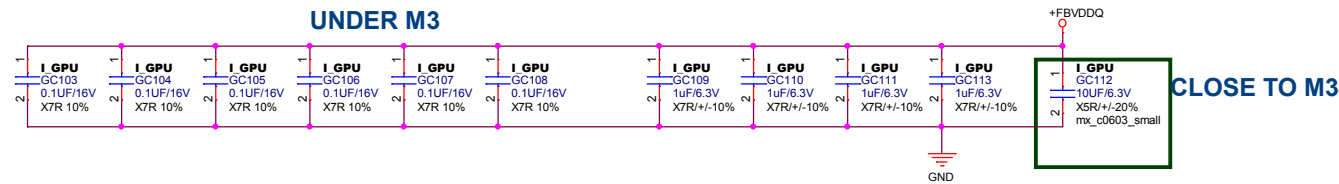
UNDER M1



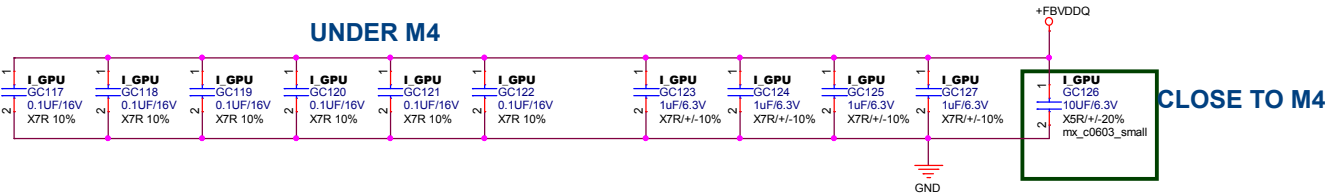
UNDER M2



UNDER M3

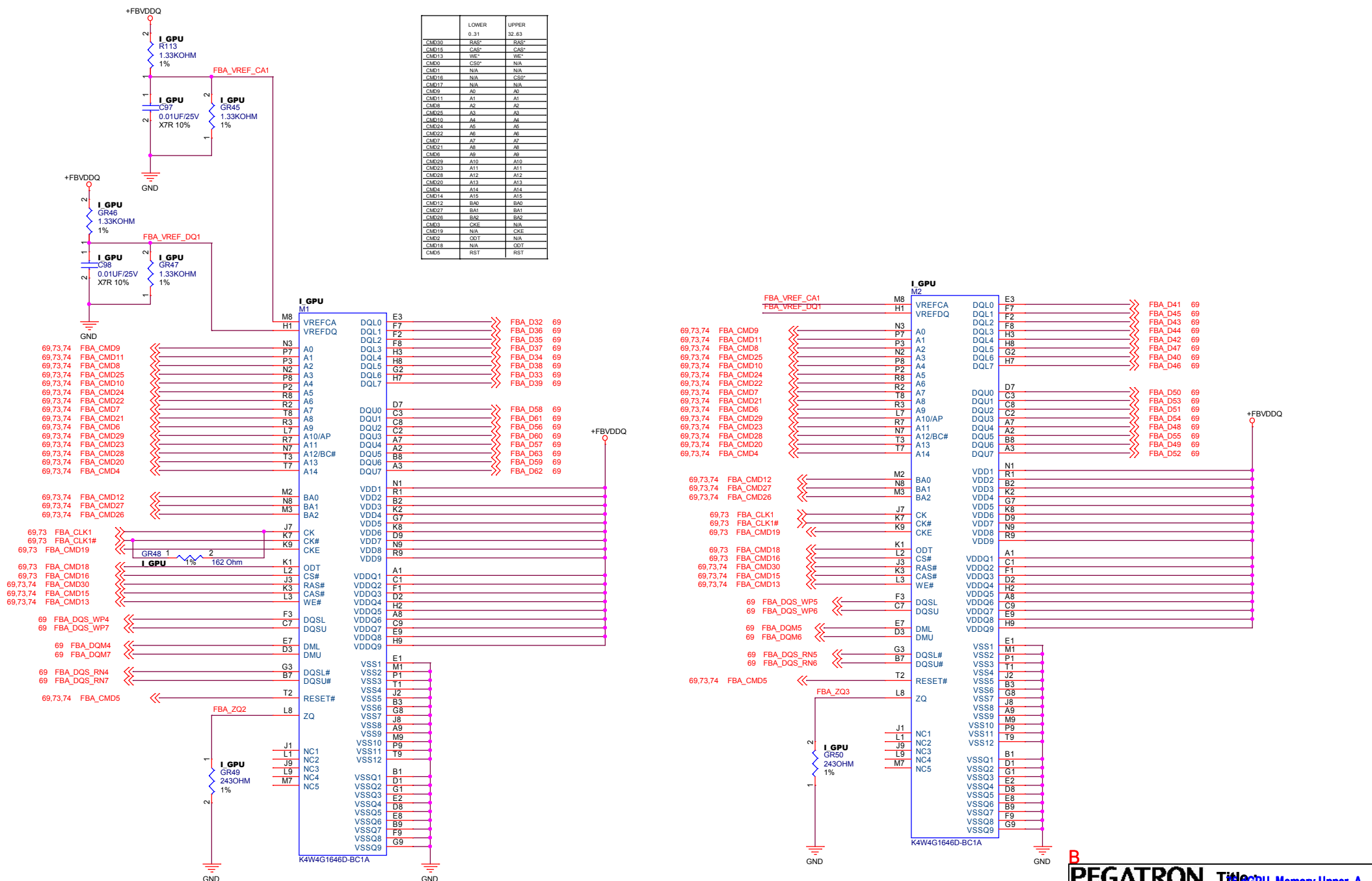


UNDER M4

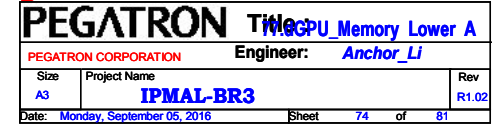


## Memory Upper Partition A

|       | LOWER            | 0.31             | UPPER            |
|-------|------------------|------------------|------------------|
| CM050 | RAS <sup>a</sup> | RAS <sup>a</sup> | RAS <sup>a</sup> |
| CM016 | CAS <sup>b</sup> | CAS <sup>b</sup> | CAS <sup>b</sup> |
| CM013 | WE <sup>c</sup>  | WE <sup>c</sup>  | WE <sup>c</sup>  |
| CM001 | CSP <sup>d</sup> | N/A              | N/A              |
| CM001 | N/A              | N/A              | N/A              |
| CM016 | N/A              | CSP <sup>d</sup> | N/A              |
| CM019 | A2               | A2               | A2               |
| CM019 | A2               | A2               | A2               |
| CM011 | A1               | A1               | A1               |
| CM008 | A3               | A3               | A3               |
| CM001 | A3               | A3               | A3               |
| CM010 | A4               | A4               | A4               |
| CM024 | A5               | A5               | A5               |
| CM022 | A6               | A6               | A6               |
| CM022 | A7               | A7               | A7               |
| CM021 | A8               | A8               | A8               |
| CM001 | A9               | A9               | A9               |
| CM029 | A10              | A10              | A10              |
| CM023 | A11              | A11              | A11              |
| CM028 | A12              | A12              | A12              |
| CM020 | A13              | A13              | A13              |
| CM004 | A14              | A14              | A14              |
| CM014 | A15              | A15              | A15              |
| CM012 | B0               | B0               | B0               |
| CM027 | BA1              | BA1              | BA1              |
| CM026 | B02              | B02              | B02              |
| CM003 | CKA              | CKA              | CKA              |
| CM019 | N/A              | CKE              | N/A              |
| CM02  | ODT              | N/A              | N/A              |
| CM018 | N/A              | ODT              | N/A              |
| CM025 | RST              | RST              | RST              |



|      | LOWER<br>6-31 | UPPER<br>32-63 |
|------|---------------|----------------|
| CM00 | RAS*          | RAS*           |
| CM05 | CAS*          | CAS*           |
| CM13 | WE*           | WE*            |
| CM14 | NA            | NA             |
| CM17 | CST*          | CST*           |
| CM18 | NA            | CSC*           |
| CM19 | NA            | NA             |
| CM29 | AO            | AO             |
| CM31 | A1            | A1             |
| CM32 | A2            | A2             |
| CM35 | A3            | A3             |
| CM40 | A4            | A4             |
| CM45 | A5            | A5             |
| CM52 | A6            | A6             |
| CM7  | A7            | A7             |
| CM01 | A8            | A8             |
| CM06 | A9            | A9             |
| CM29 | A10           | A10            |
| CM33 | A11           | A11            |
| CM41 | A12           | A12            |
| CM49 | A13           | A13            |
| CM04 | A14           | A14            |
| CM15 | A15           | A15            |
| CM12 | BAO           | BAO            |
| CM27 | BA1           | BA1            |
| CM08 | BA2           | BA2            |
| CM3  | CKE           | NA             |
| CM19 | NA            | CKE            |
| CM20 | COT           | NA             |
| CM18 | NA            | COT            |
| CM5  | RST           | RST            |





BIOS, External SS, and Mechanical Components

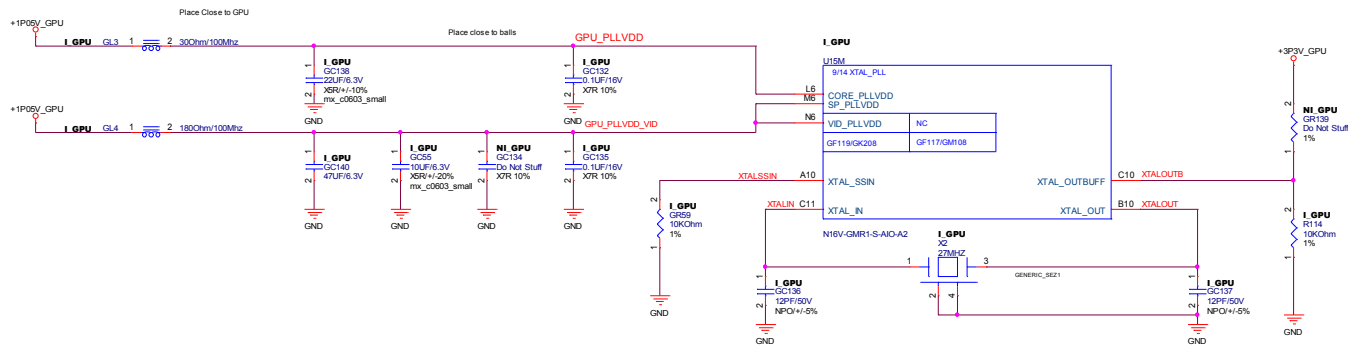
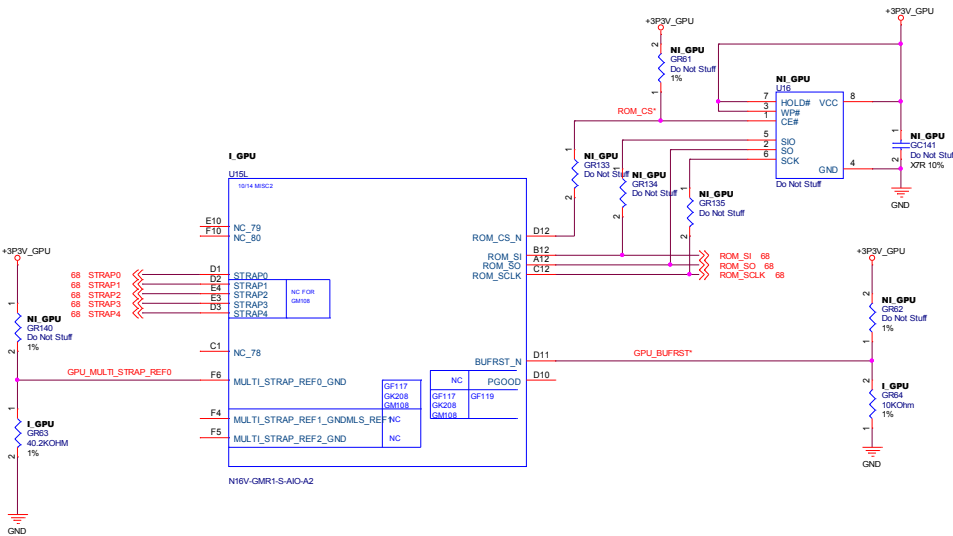


Table 119. Device Specific Strap Mode Selection

|  | N14M-GE/-GL | Other N14x GPUs |
|--|-------------|-----------------|
| Multi_Strap_Ref2_GND<br>(Only on GB2-64 package) | No Connect  | N/A             |
| Multi_Strap_Ref1_GND<br>(Only on GB2-64 package) | No Connect  | N/A             |
| Multi_Strap_Ref0_GND                             | No Connect  | 40.2k 1% to GND |
| Strap Mode Selected                              | Binary      | Multi-Level     |

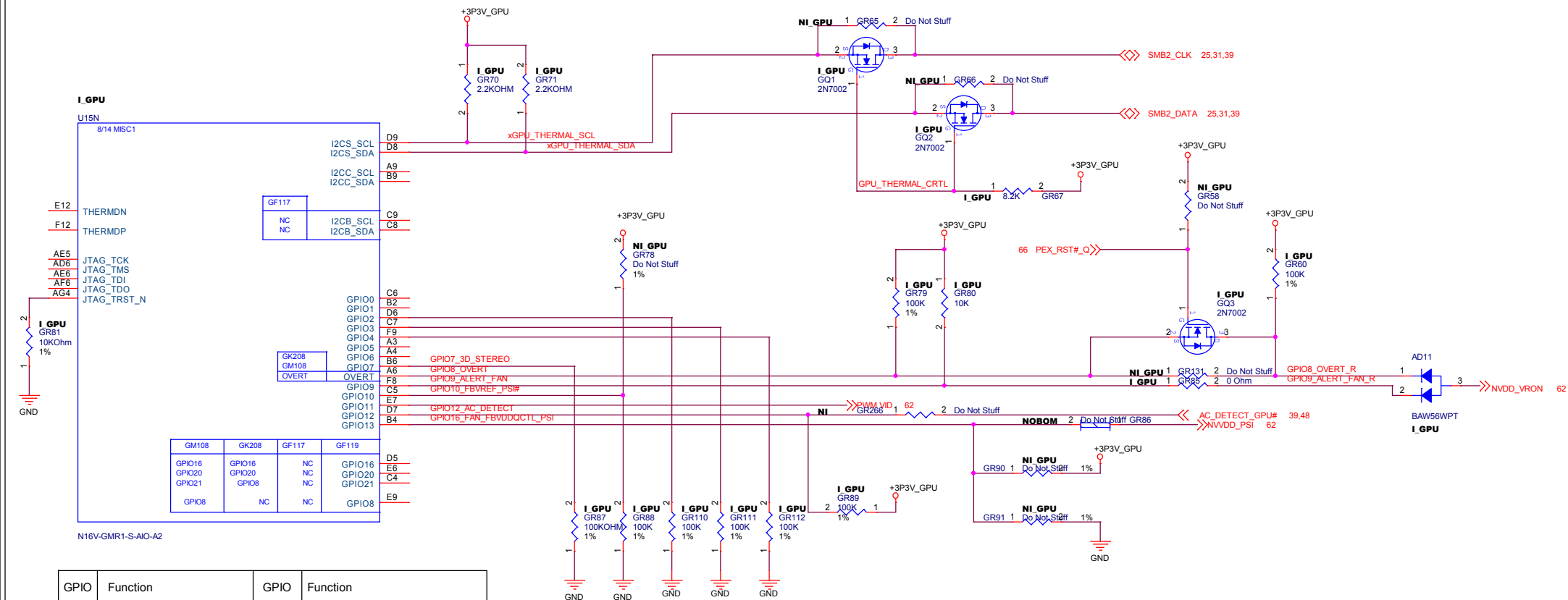
STUFF PDs on XTALSSIN and  
XTALOUTBUFF WHEN EXT\_SS  
IS NOT USED

BIOS ROM



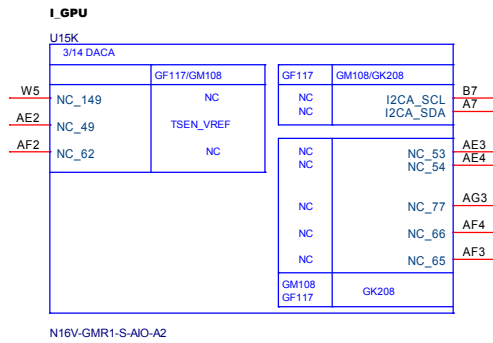
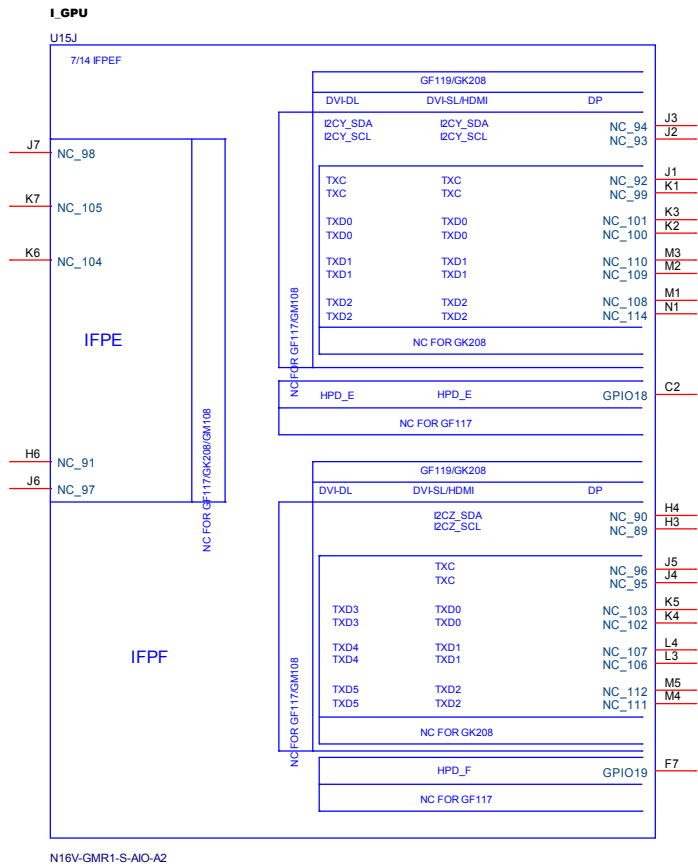
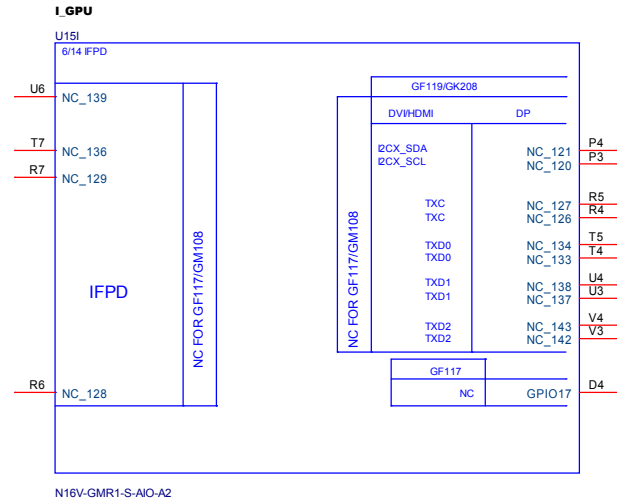
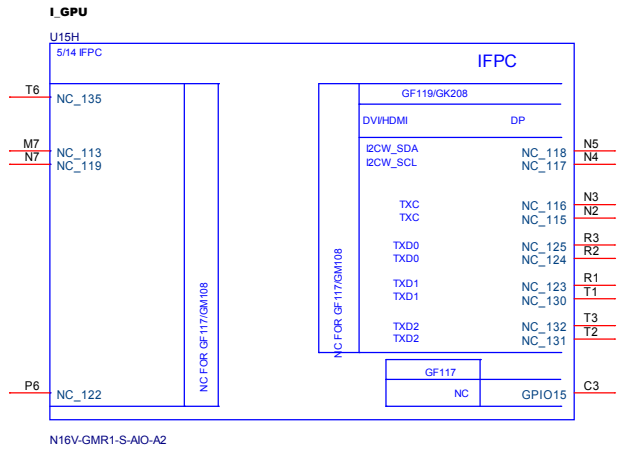
R1.01-2011/12/22:  
Add R37589 to pull down;  
R37586 change to "NI".

## GPIOs, Thermal Sensor, I2C/GPIO Expanders

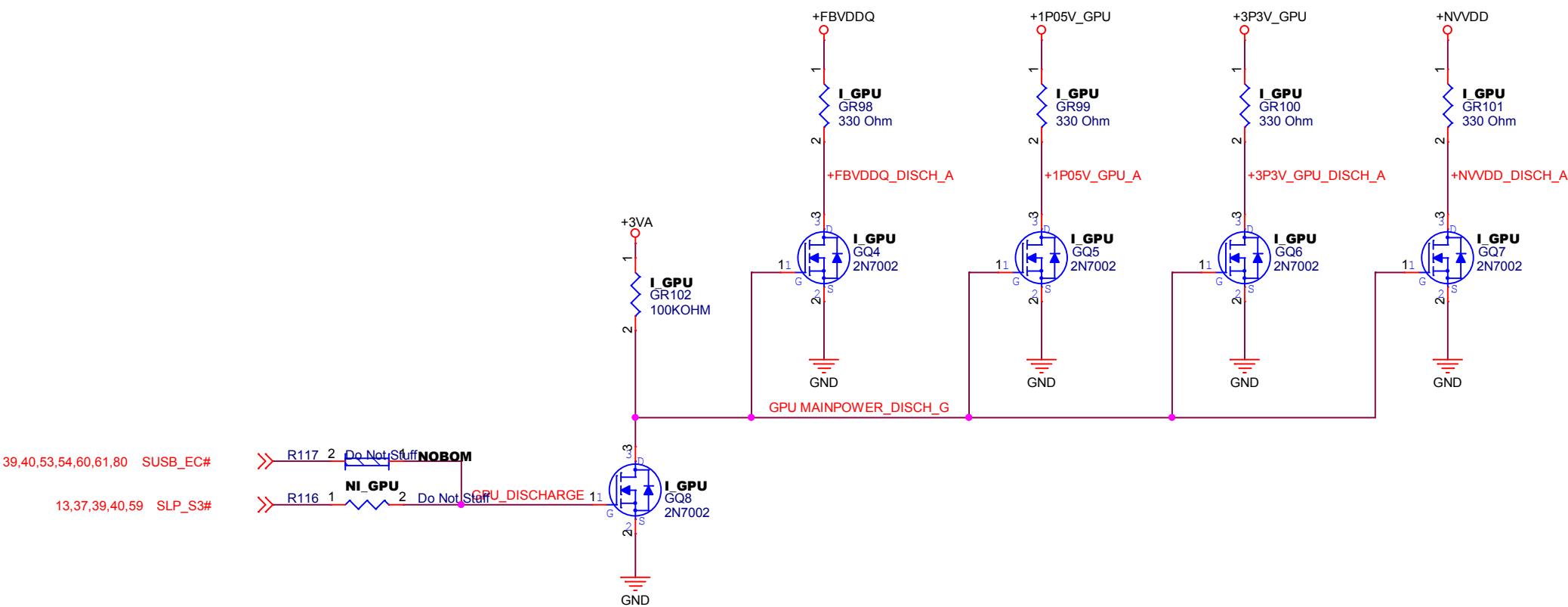


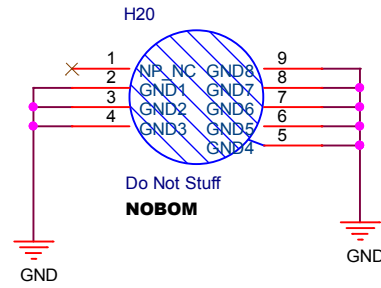
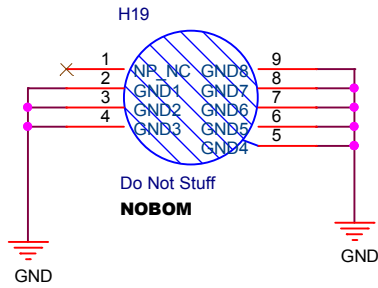
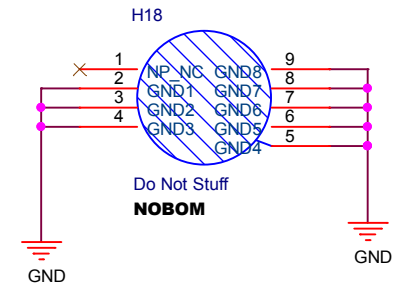
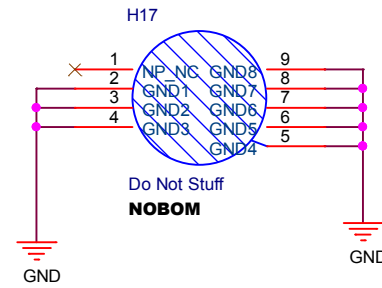
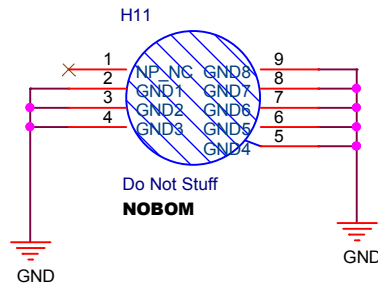
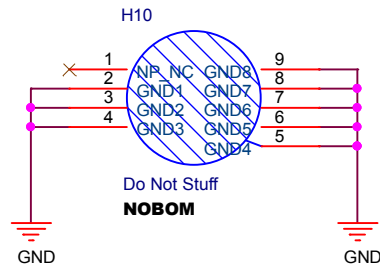
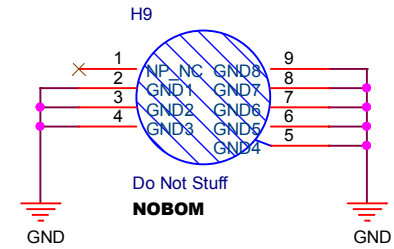
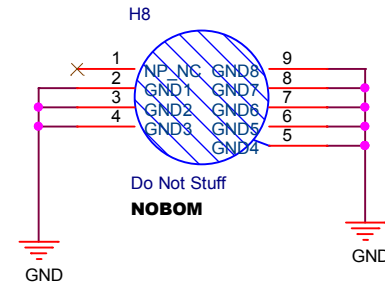
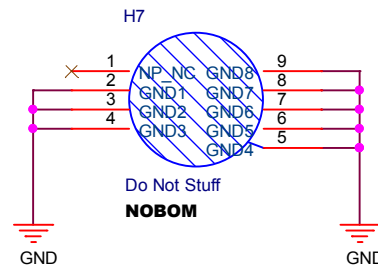
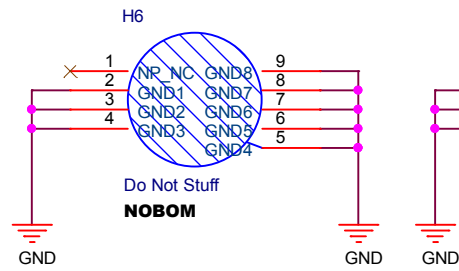
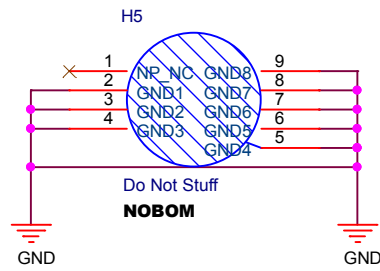
| GPIO    | Function                         | GPIO    | Function                       |
|---------|----------------------------------|---------|--------------------------------|
| GPIO 0  | Debug/Service Header/Alt_Fan PWM |         | I2C PORT C                     |
| GPIO 1  | VID 2                            | EXPND 0 | Level Shifter Error Correction |
| GPIO 2  | LCD brightness control (BL PWM)  | EXPND 1 | NVGEM GPIO EXP1/ PS_Margin*    |
| GPIO 3  | LCD Power enable (PPEN)          | EXPND 2 | NVGEM GPIO EXP2/PS_MR*         |
| GPIO 4  | LCD Backlight enable (BLEN)      | EXPND 3 | GPIO_DEBUG_SERVICE HEADER      |
| GPIO 5  | VID 0                            |         |                                |
| GPIO 6  | VID 1                            |         |                                |
| GPIO 7  | 3D STEREO                        |         | SMBUS                          |
| GPIO 8  | GPU Overtemp                     | EXPND 4 | GPU_PS_EN                      |
| GPIO 9  | GPU thermal Alert                | EXPND 5 | RSVD                           |
| GPIO 10 | FB Vref Control (not used sDDR3) | EXPND 6 | PEX_RST                        |
| GPIO 11 | FBVDD/Q VID (Reserved)           | EXPND 7 | RSVD                           |
| GPIO 12 | PWR_Level AC Detect              |         |                                |
| GPIO 13 | PS1 Vprgm Enable                 |         |                                |
| GPIO 14 | HPD for IFP AB (not used)        |         |                                |
| GPIO 15 | HPD for IFP C (HDMI/DP)          |         |                                |
| GPIO 16 | Fan PWM control                  |         |                                |
| GPIO 17 | HPD for IFP D (DP)               |         |                                |
| GPIO 18 | HPD for IFP E (DVI-I DL)         |         |                                |
| GPIO 19 | HPD for IFP F (not used)         |         |                                |
| GPIO 20 | NVGEM Debug GPIO13               |         |                                |
| GPIO 21 | NVGEM Debug GPIO14               |         |                                |

## IFPD DUAL MODE DP HDMI DVI



# GPU POWER DISCHARGE

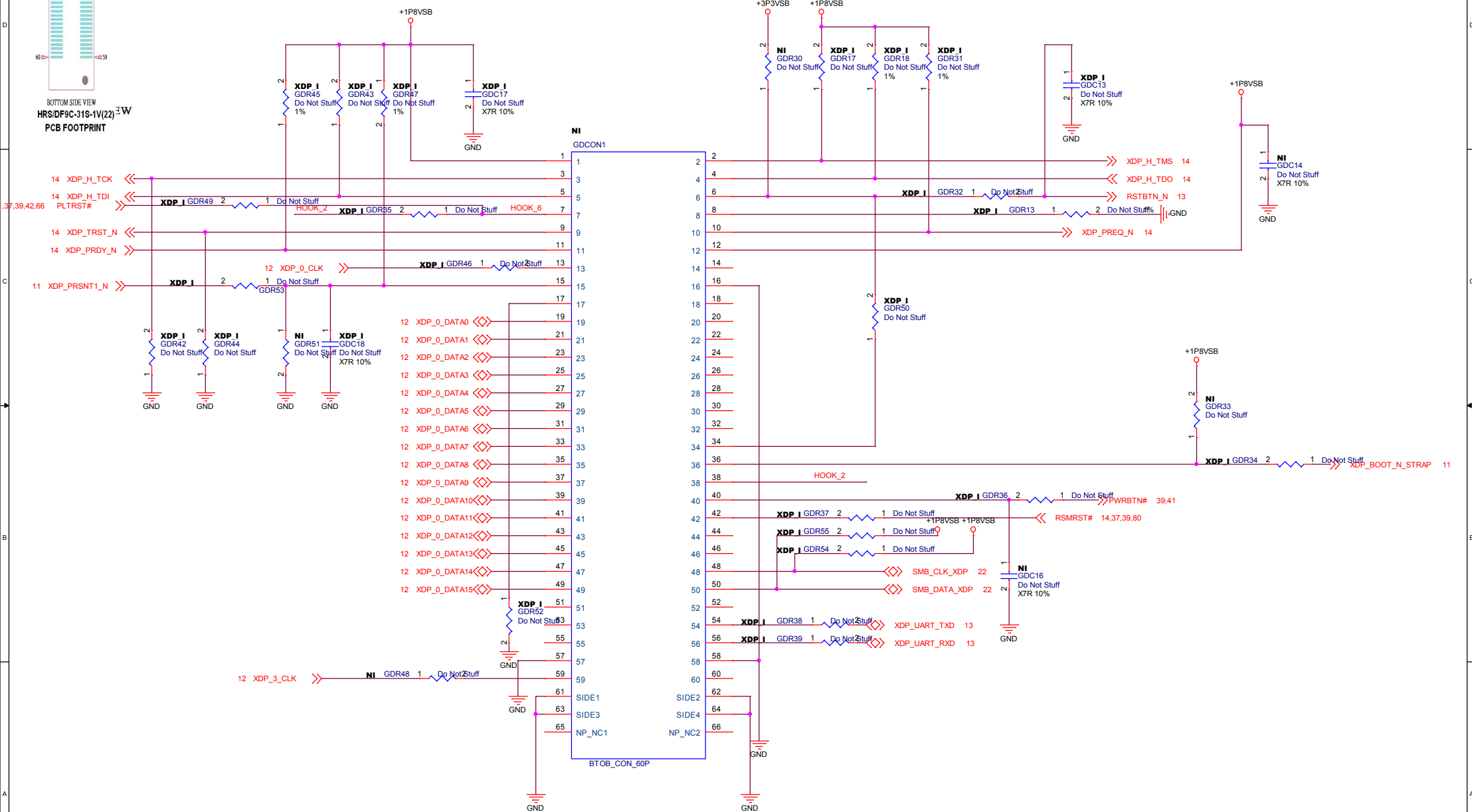






## INTEL CPU XDP DEBUG PORT

XDP change part to 1216-016H000



|                      |                                  |                  |    |                           |              |
|----------------------|----------------------------------|------------------|----|---------------------------|--------------|
| <b>B</b>             |                                  | <b>PEGATRON</b>  |    | <b>Title :</b> 85.CPU XDP |              |
| PEGATRON CORPORATION |                                  | <b>Engineer:</b> |    | Anchor_Li                 |              |
| Size<br>A3           | Project Name<br><b>IPMAL-BR3</b> |                  |    |                           | Rev<br>R1.02 |
| Date:                | Monday, September 05, 2016       | Sheet            | 81 | of                        | 81           |